Embedded and ambient systems - final exam

Time available: 60 minutes
Maximal score: 20 points
Required score to pass: 10 points

1.	Sketch the architecture of the flash ADC. How many resistors are required in an N bit ADC?	2 points
2.	Sketch the architecture of 3 bit Bit-per-Stage ADC consisting MagAmp stages! Sketch also the architecture of the MagAmp stage!	2 points
3.	Sketch the architecture of an R-2R ladder type DAC, which provides voltage output from voltage reference.	2 points
4.	Sketch the transfer function (amplitude specification) of a cascaded decimation filter, where the first stage has a decimation factor of 3, the second stage a decimation factor of 2. Take care not to give an unnecessarily strict specification at the first stage, knowing that the second stage will filter out certain part of the spectrum. Scale the frequency axis with the corresponding sampling frequency.	2 points
5.	Sketch the transfer function (amplitude specification) of a factor 4 interpolation filter (inserting zeros between samples + lowpass filtering) in the range of 0..f_s, where f_s is the new sampling frequency. What is the amplitude specification at $f_s/16$, $f_s/8$, $f_s/4$ and $f_s/2$?	2 points
6.	How the Signal to Noise and Distortion Ratio is defined (measuring the dynamic properties of ADCs)? Provide the formula, and the meaning of the variables in the formula.	2 points
7.	Sketch the interconnection of 1 master and 3 slaves trough SPI interface, where the master wants to write different messages to the different slaves, but there is only one Slave Select pin (and you are not allowed to use any further general purpose IO pin for that purpose). Denote at the nodes the name of the wires from the point of view of that particular node (let it be unambiguous what is input and what is output at the particular node).	2 points
8.	How is in the FlexRay protocol the fault-tolerant behavior assured by choosing appropriate bus topology? Sketch one possible topology and explain how the fault-tolerance is assured.	2 points
9.	How can we generate N* f_0 frequency from f_0 frequency using PLL? Sketch the architecture.	2 points
10.	Sketch the architecture of the Address generator arithmetic, which calculates the address in a circular buffer. Denote the base address with B, the buffer length with L, the index within the buffer wit I, and the step size by M.	2 points