Embedded and ambient systems - final exam

Time available: 60 minutes
Maximal score: 20 points
Required score to pass: 10 points

1.	Sketch the architecture of the Address generator arithmetic, which calculates the address in a circular buffer. Denote the base address with *B*, the buffer length with *L*, the index within the buffer wit *I*, and the step size by *M*.	2 points
2.	What are the fundamental possibilities to increase the speed of processing units (microcontrollers, DSPs, processors etc.)? Enumerate at least 3. Which one is used among these in enhanced traditional DSPs which is not characteristic to traditional DSPs.	2 points
3.	Sketch the architecture of 3 bit Bit-per-Stage ADC consisting MagAmp stages! Sketch also the architecture of the MagAmp stage!	2 points
4.	Sketch the architecture of subranging ADC! Draw the logical block diagram and explain its working principle with few sentences.	2 points
5.	Sketch the amplitude specification of a factor 3 decimation filter in the frequency range of 0 .. fs, where fs is the sampling frequency. What is the amplitude specification at $f_s/12$, $f_s/6$, $f_s/2$ and $5f_s/6$?	2 points
6.	Sketch the architecture of the Kelvin-Varley segmented DA structure! How many resistors are needed for a 14 bit DAC if you have 7+7 bit segments? How many would be needed for a string type DAC?	2 points
7.	Sketch the architecture of a Sigma-Delta DAC (the whole DAC, not only the modulator!). Denote at each input and output of the blocks, whether the signal is analog (A) or digital (D). If digital, denote the bit number and sampling frequency. (At the input of the DAC let the bit number be N, and the sampling frequency f_s.)	2 points
8.	Outline the arbitration mechanism at I^2C bus. Draw the logic states of the following lines as a function of time: SDA1 forced by master1, SDA2 forced by master 2, SDA as a result of the two datalines, SCL. Denote unambiguously, what the masters monitor on the bus, and what are their reactions.	2 points
9.	Sketch the interconnection of 1 master and 3 slaves trough SPI interface, where the master wants to address each slave separately. Denote at the nodes the name of the wires from the point of view of that particular node (let it be unambiguous what is input and what is output at the particular node).	2 points
10.	How can we generate N* f_0 frequency from f_0 frequency using PLL? Sketch the architecture.	2 points