FlexRay protocol

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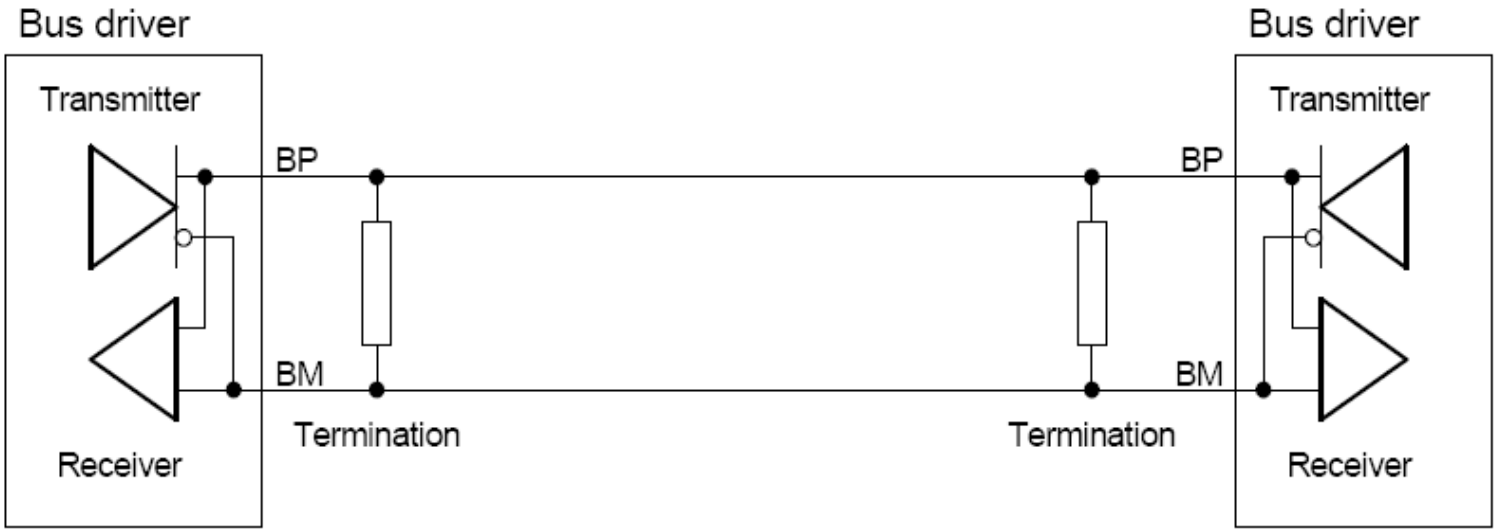
General facts

- Automotive choice for X-by-Wire applications
- Combination of time-triggered and event triggered approach
- Application in safety-critical, fault-tolerant systems
- First commercial appearance: in 2006
  - BMX-X5 active suspension, adaptive cruise control

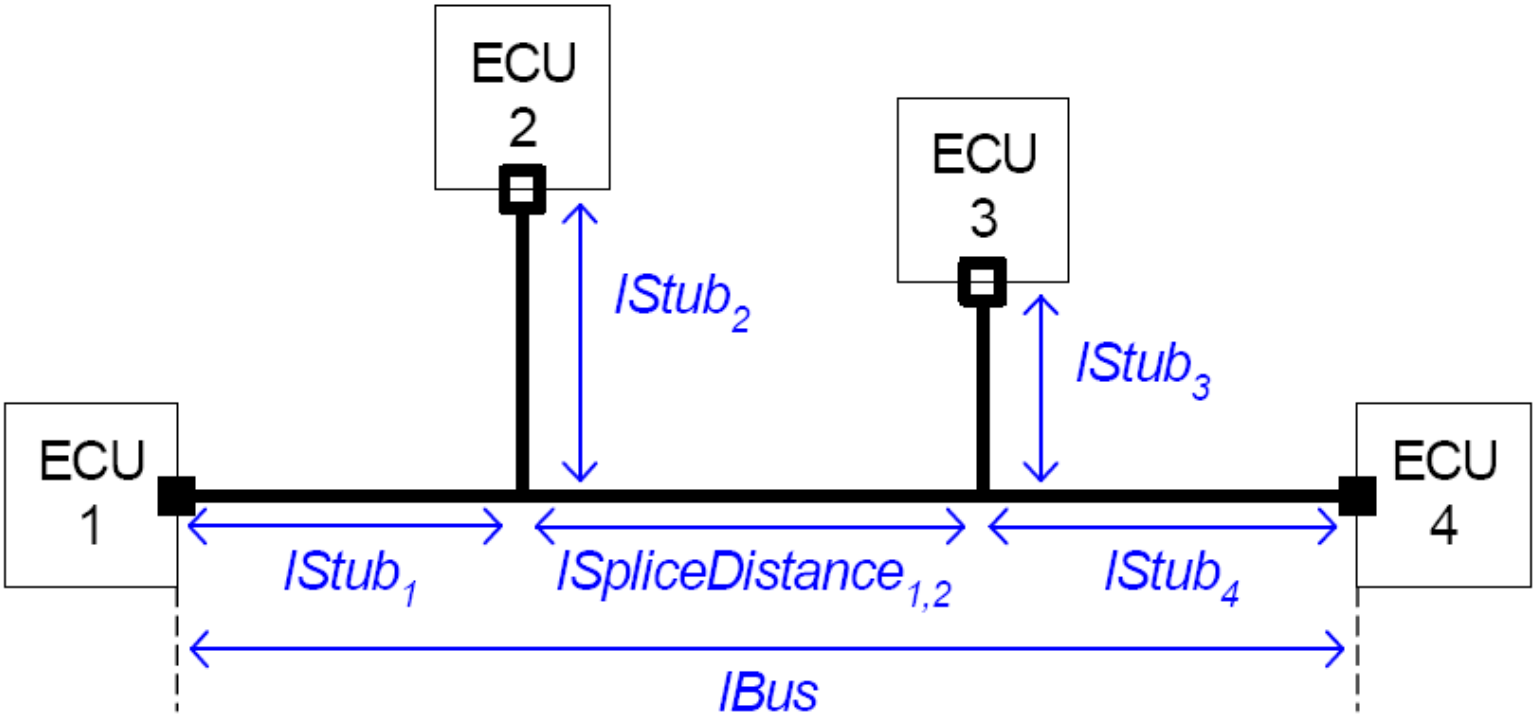
Connection of nodes

- Differential voltage
  - Bus plus (BP)
  - Bus minus (BM)

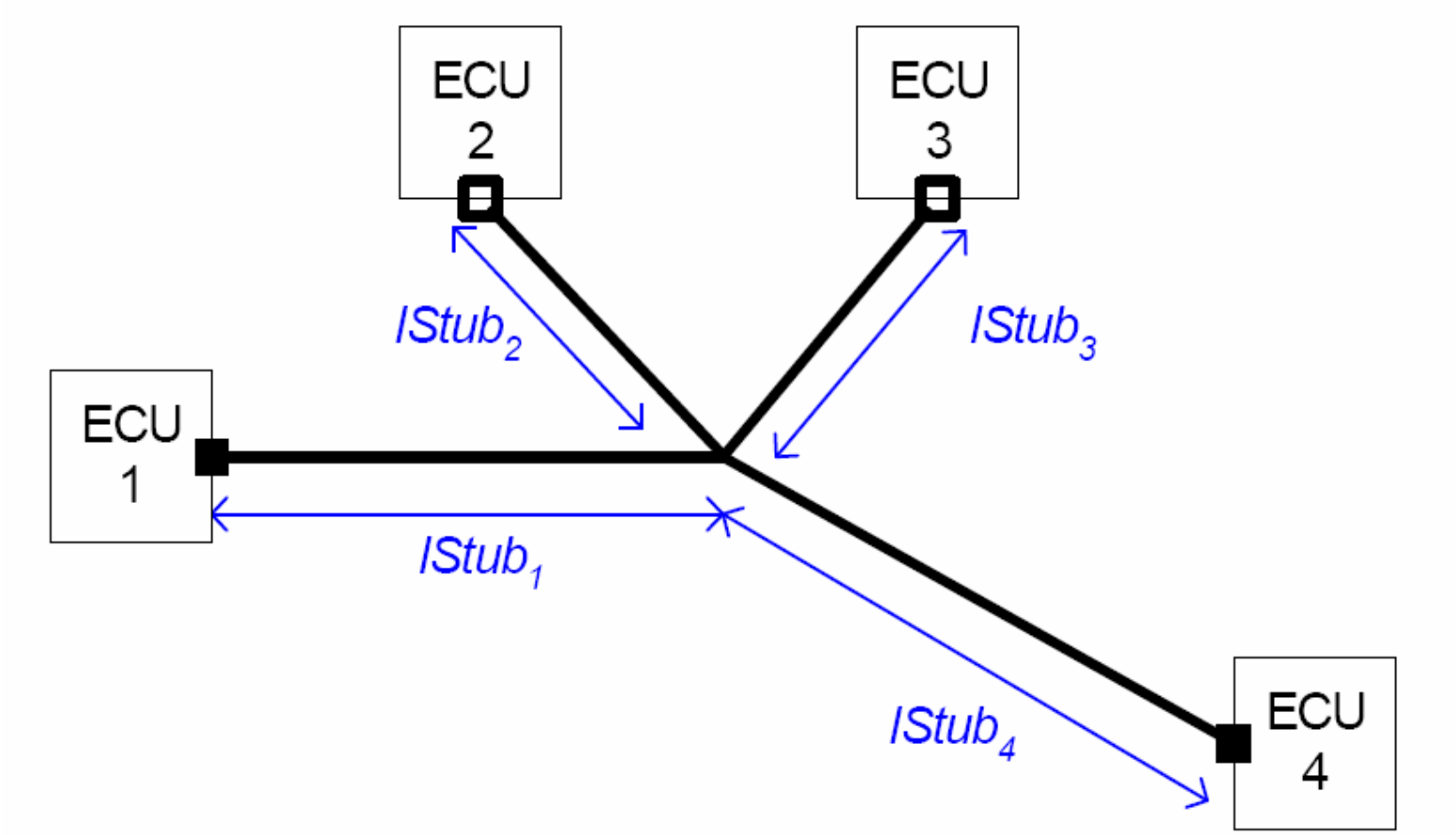


Bus topology

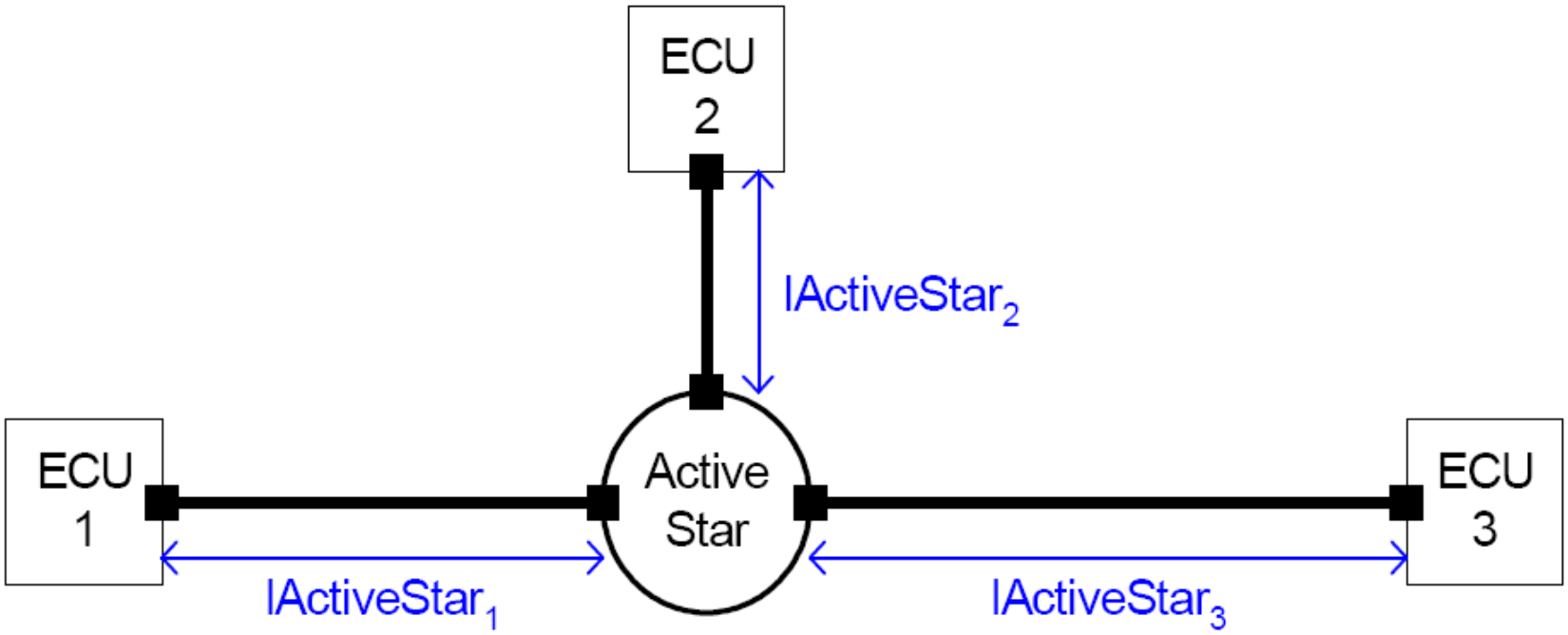
- Linear passive bus



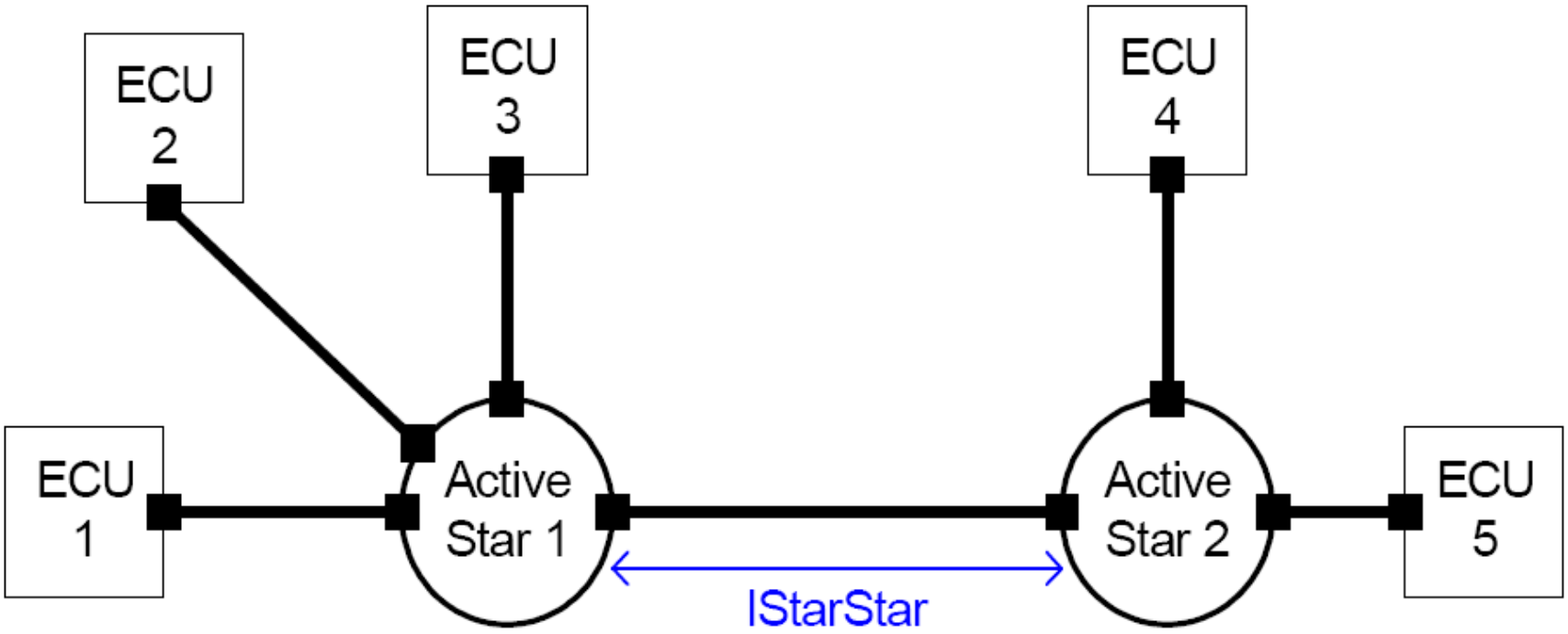
- Passive star



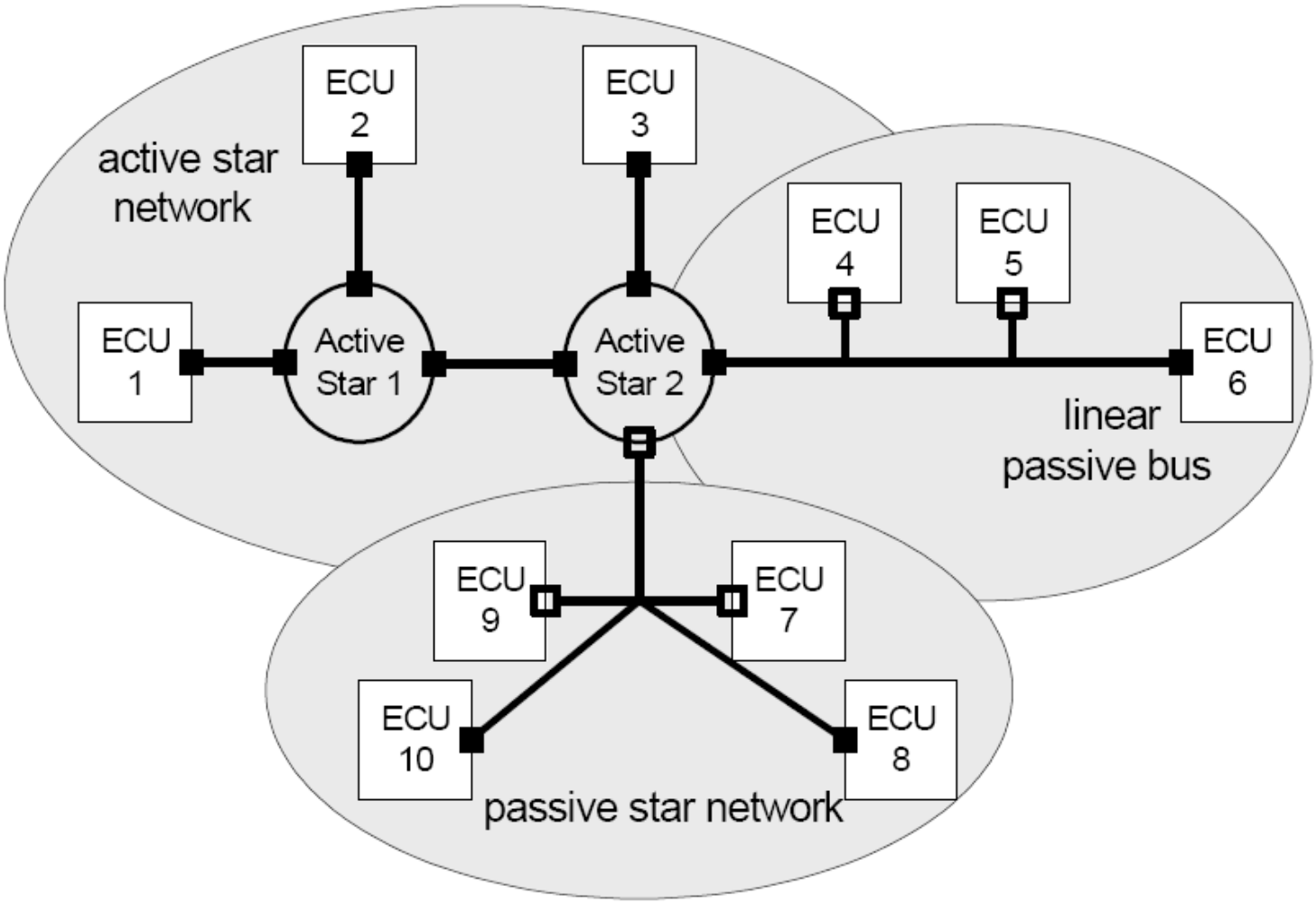
- Active star


ECU
2
IActiveStar2
ECU
1
Active
Star
ECU
3
IActiveStar1
IActiveStar3

- Single channel cascade star

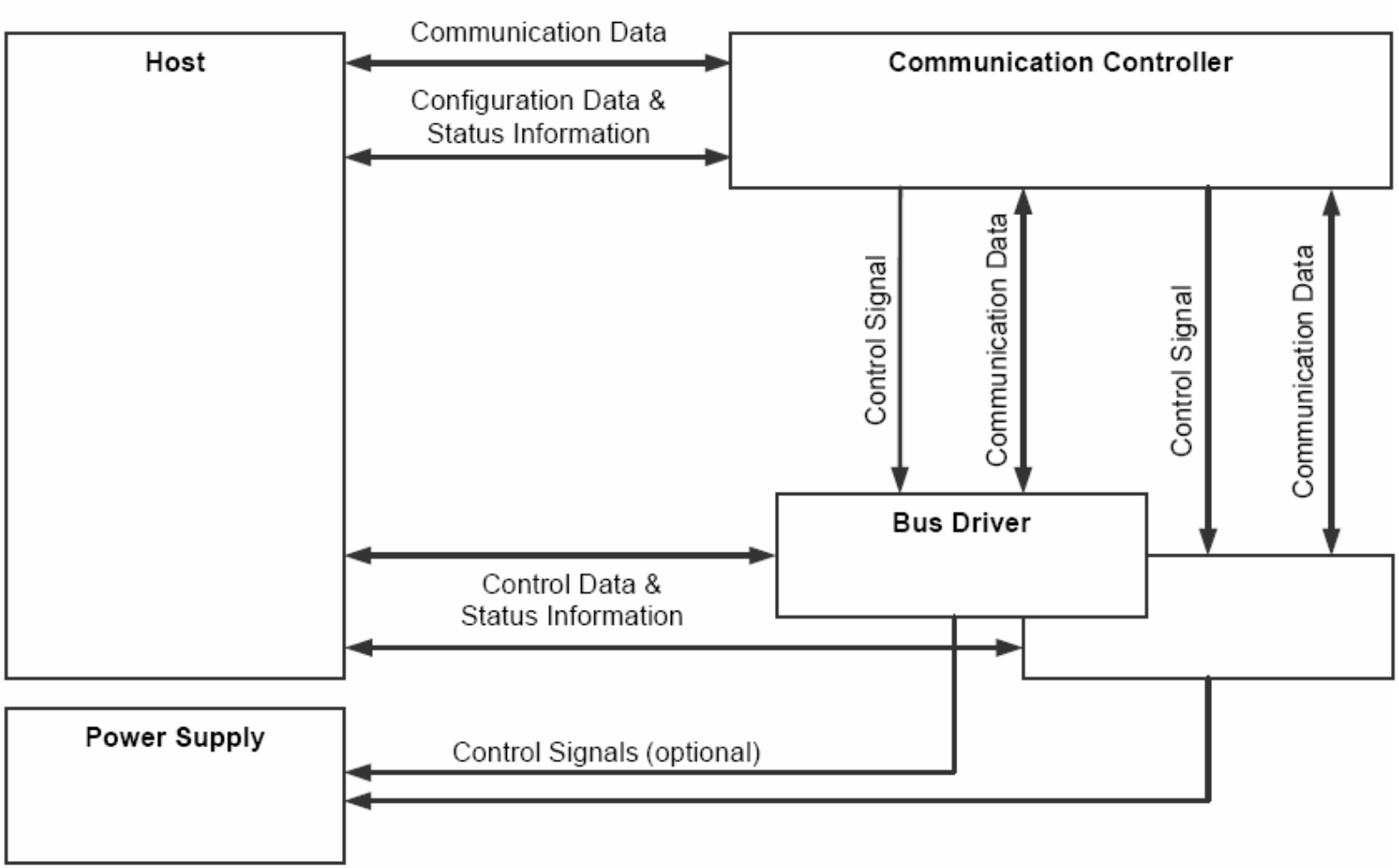


- Hybrid


ECU 2
ECU 3
active star network
ECU 4
ECU 5
ECU 1
Active Star 1
Active Star 2
ECU 6
linear passive bus
ECU 9
ECU 7
ECU 10
ECU 8
passive star network

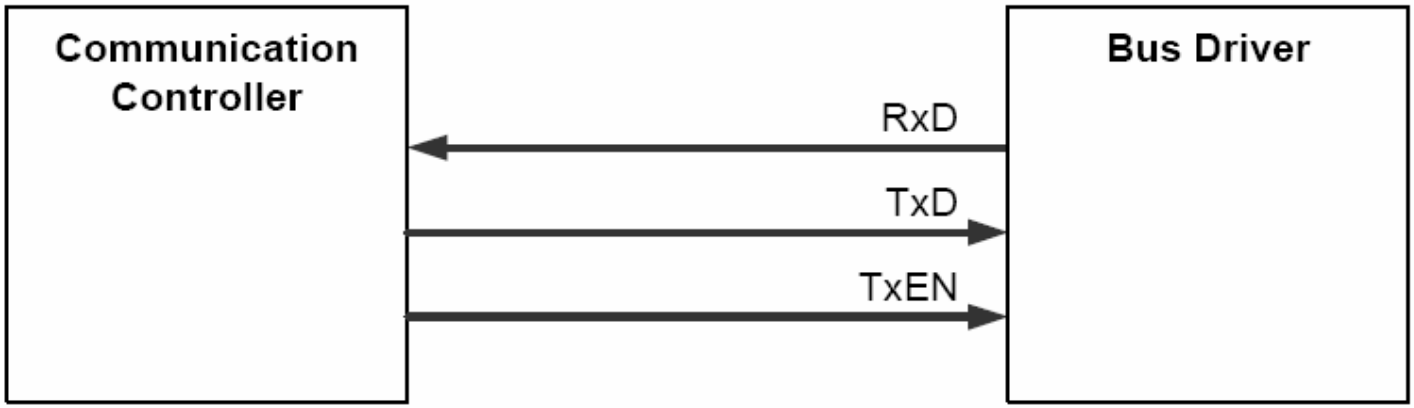
- Dual channel topologies
  - FlexRay communication modules offer the possibility to serve up to two channels
    - Increase bandwidth
    - Introduce a redundant channel in order to increase the level of fault tolerance

Node architecture

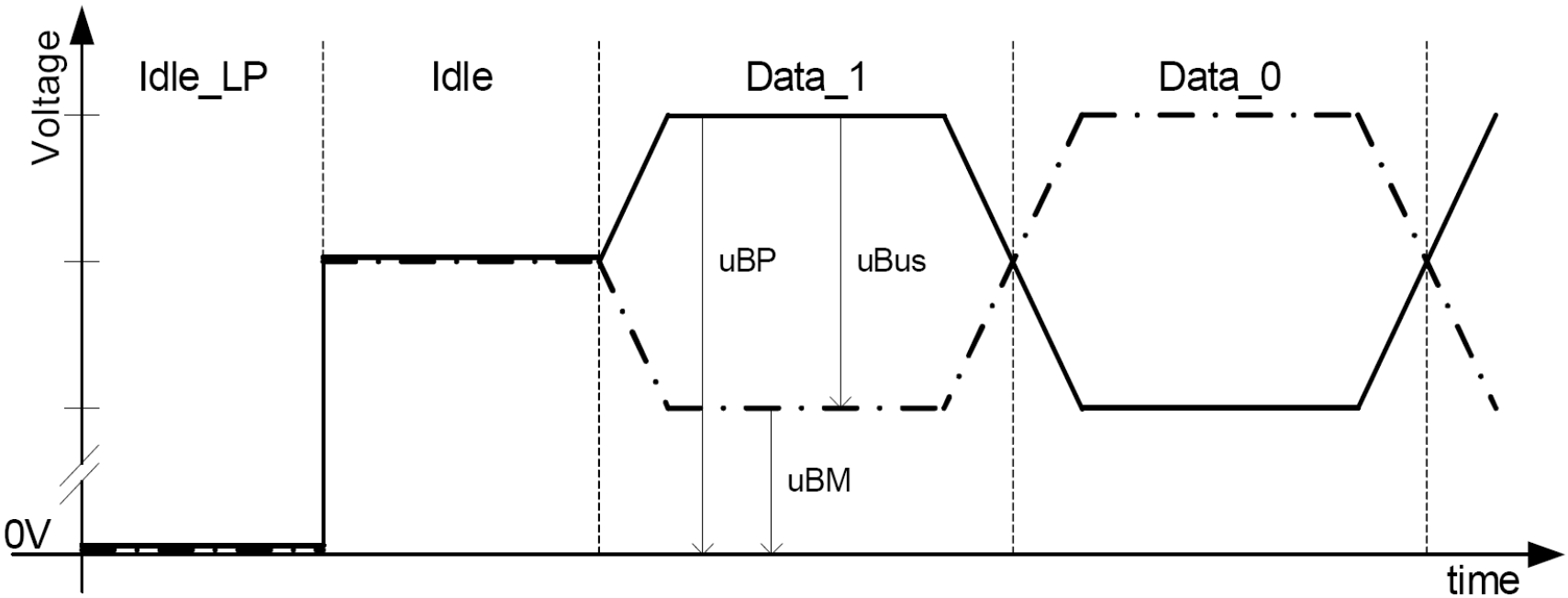


Communications controller – bus driver interface

- TxEN (Transmit Data Enable Not)
  - CC's request to have the bus driver present the data on the TxD line to its corresponding channel



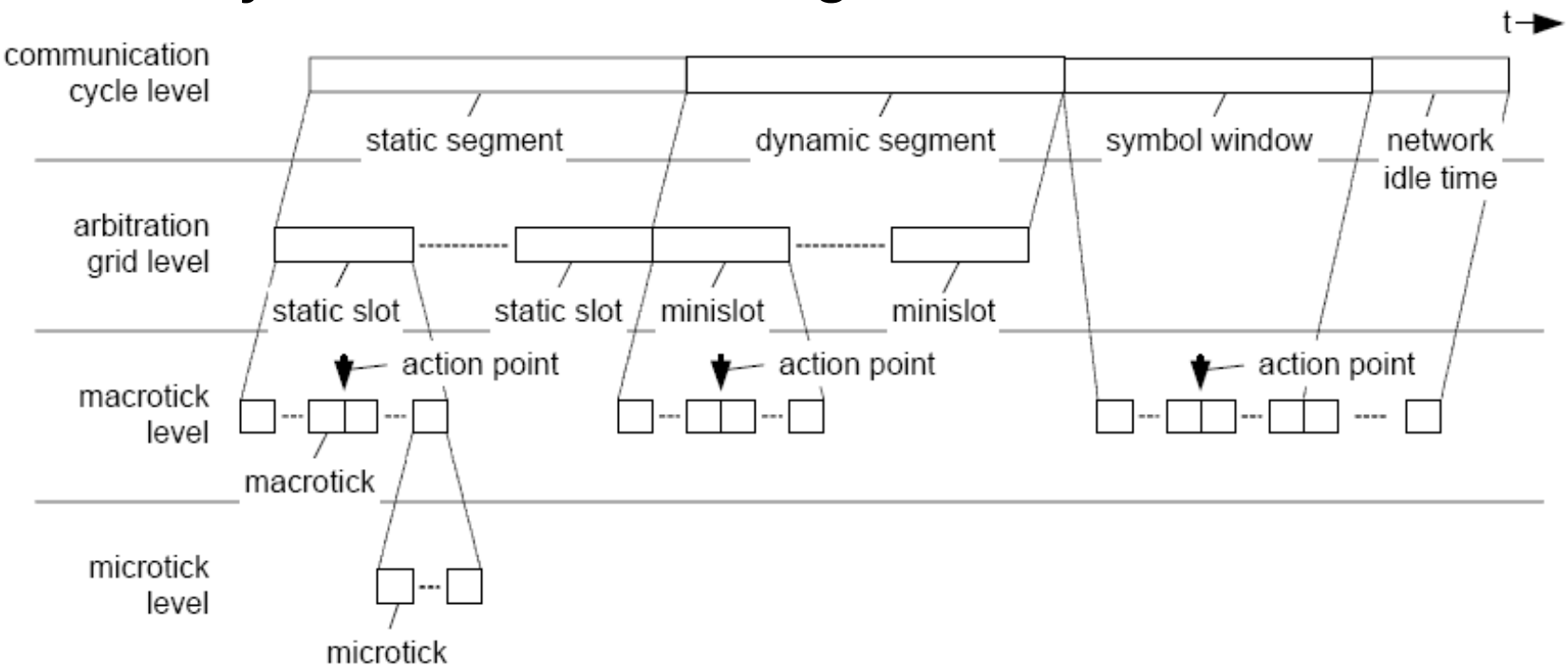
Physical layer signalling



- Differential voltage on bus is defined as uBus = uBP – uBM
- Wiring:
  - UTP or STP (unshielded or shielded twisted pair)
  - Optical

Media access control

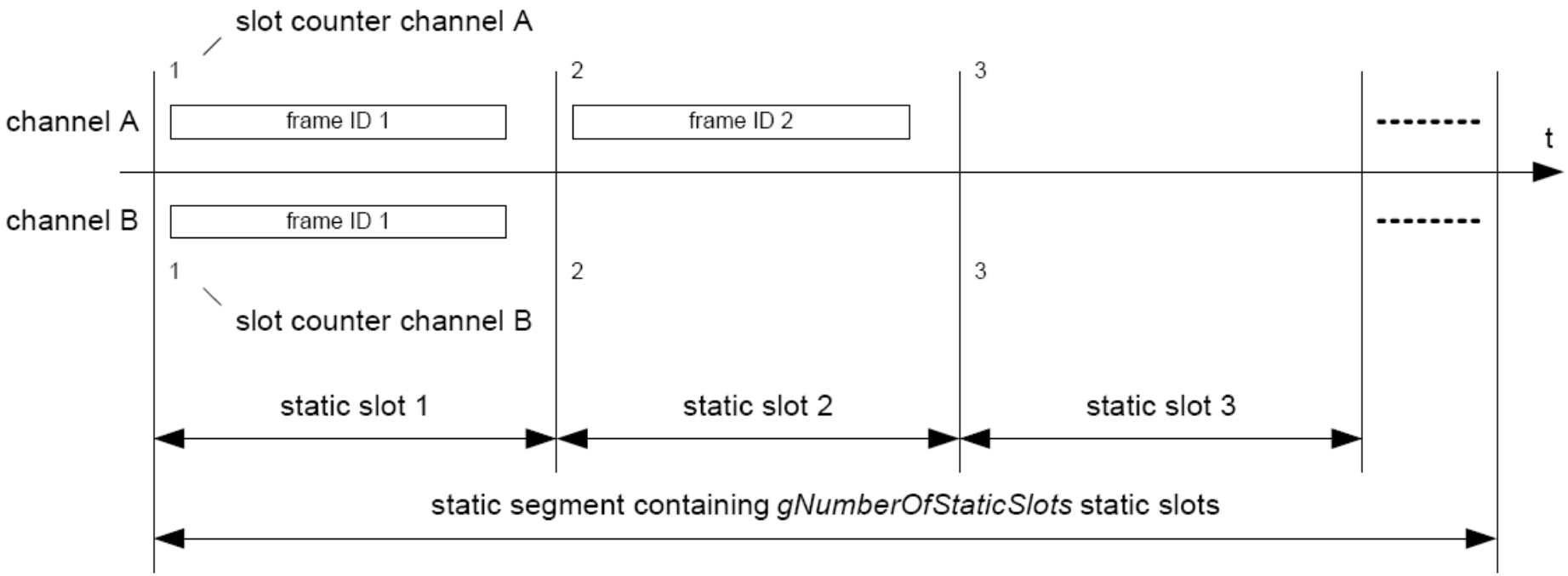
- Repeptitive communication cycles
  - TDMA (tome division multiple access)
  - Dynamic mini-slotting



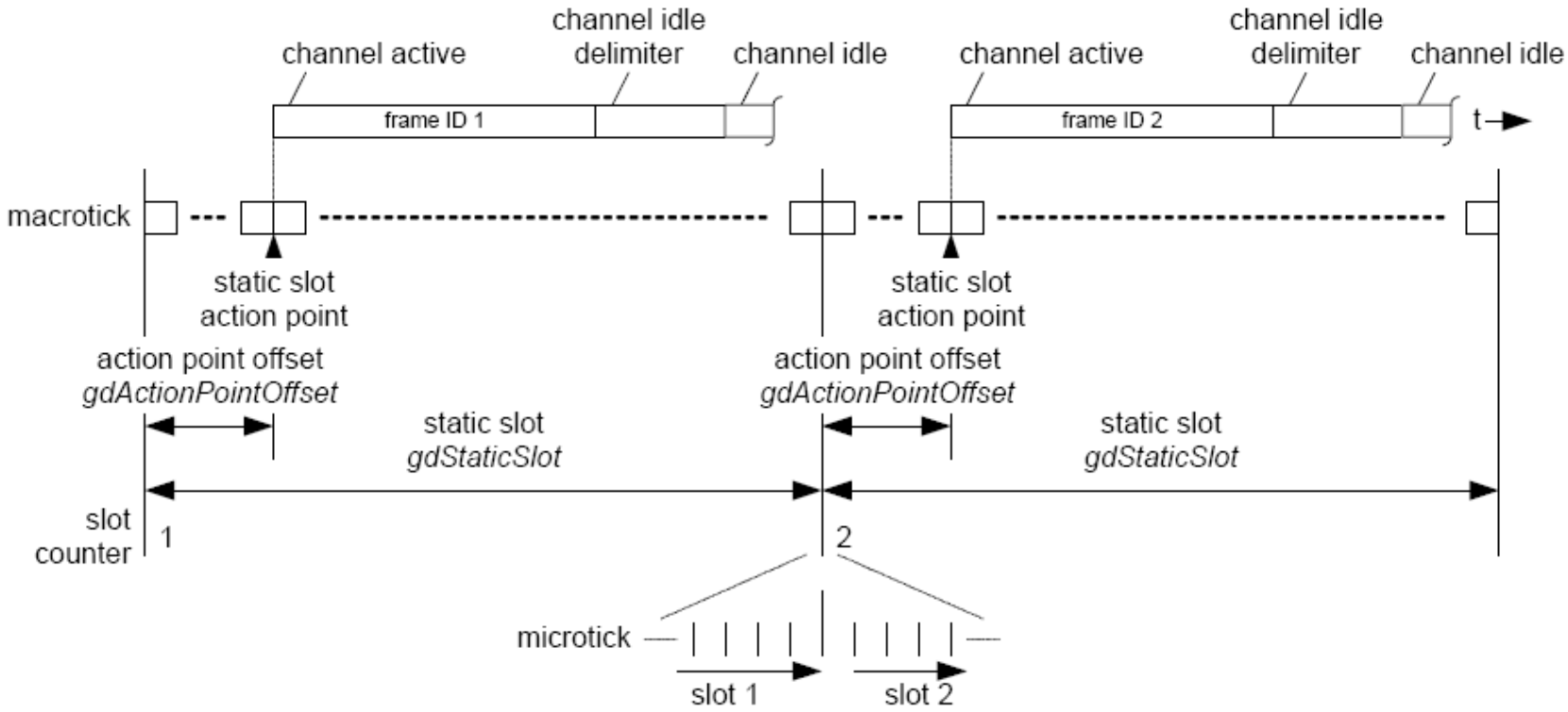
- Action point: specific instants at which transmissions shall start and shall end
- Arbitration: a certain transmitter can send data at a certain time
- Static segment and idle are mandatory
- Dynamic segment is optional

Static segment

- Every slot adn frame has the same (but configurable) length



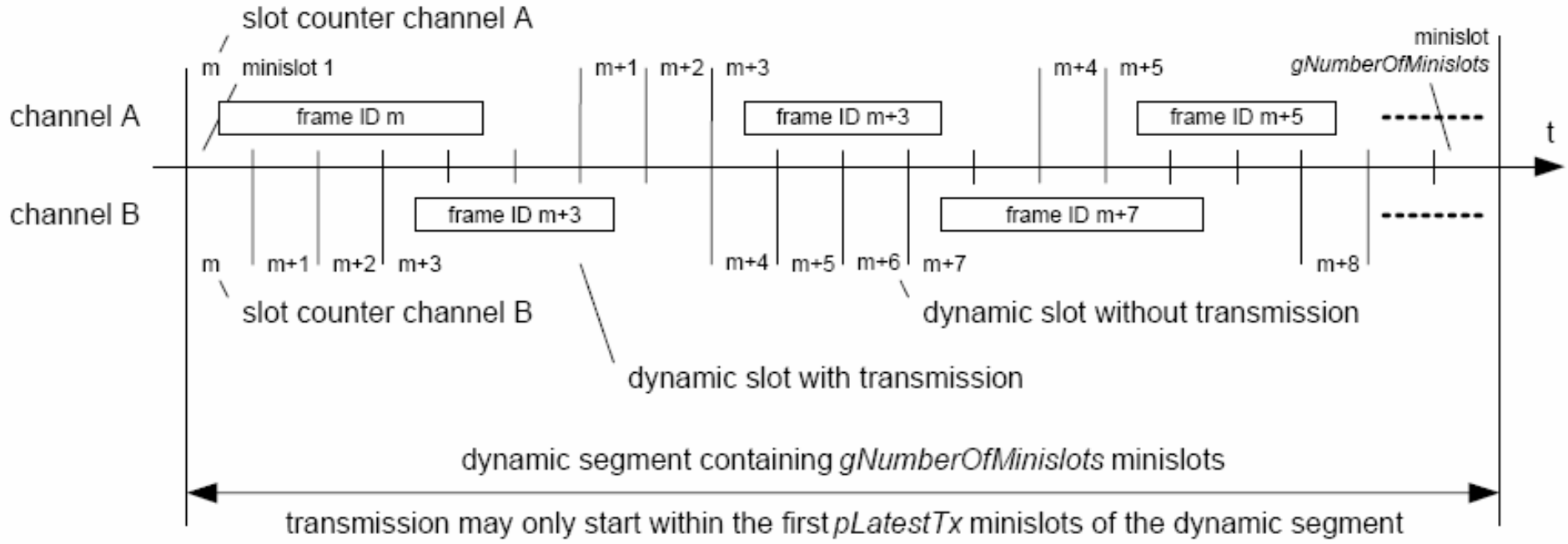
- Timing of static slot



Dynamic segment

- Frames with variable length
- Arbitration based on minislots
- The number of minislots within one claster is fixed
- Action point: start of transmission inside minislots

- Structure of dynamic segment

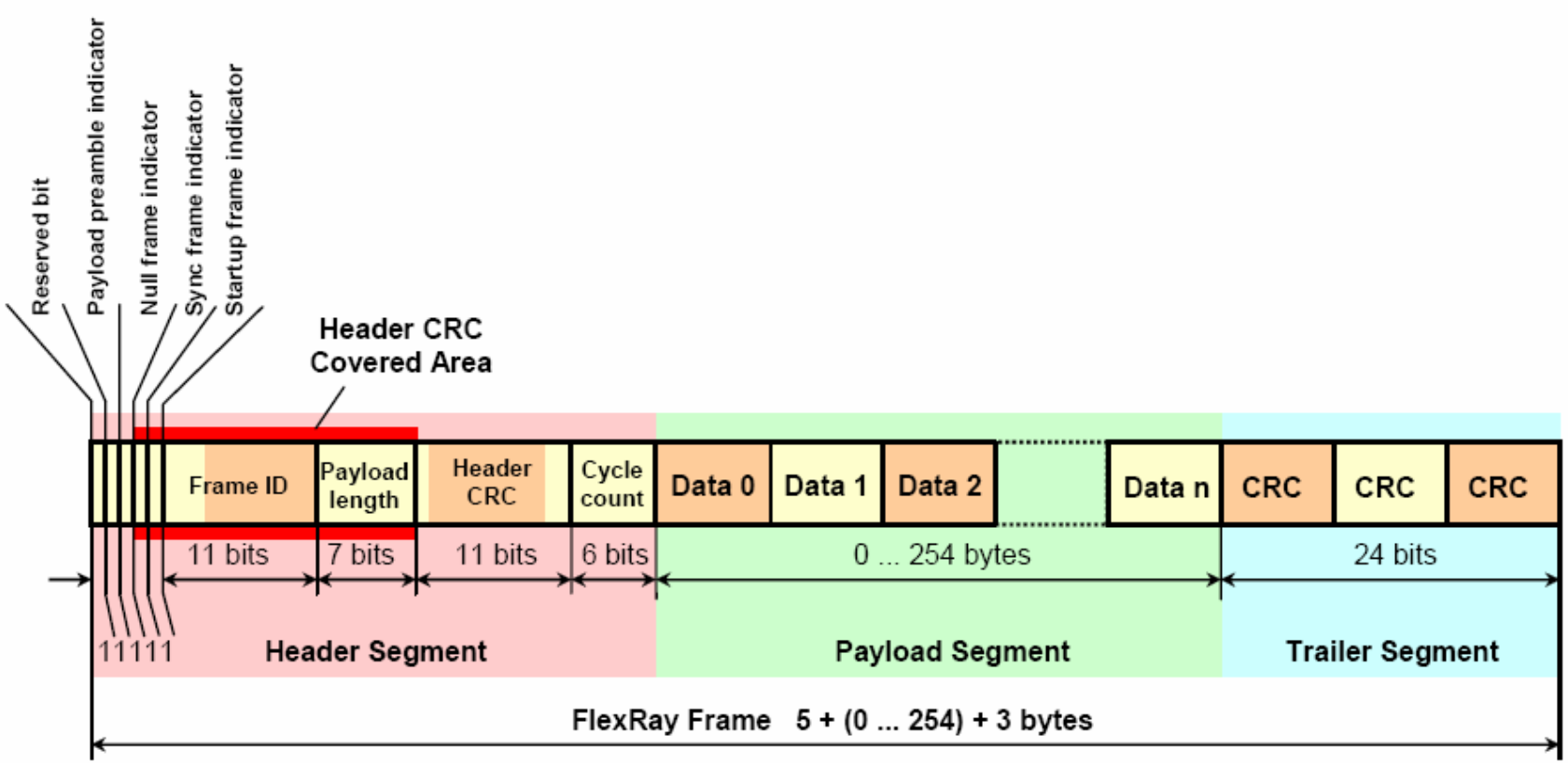


Symbol window

- One symbol can be sent in one window
- No arbitrations in the protocol
  - If still needed higher level implenetation

- Symbol
  - Collision avoidance symbol (CAS)
  - Media access test symbol (MTS)
  - Wakeup symbol (WUS)

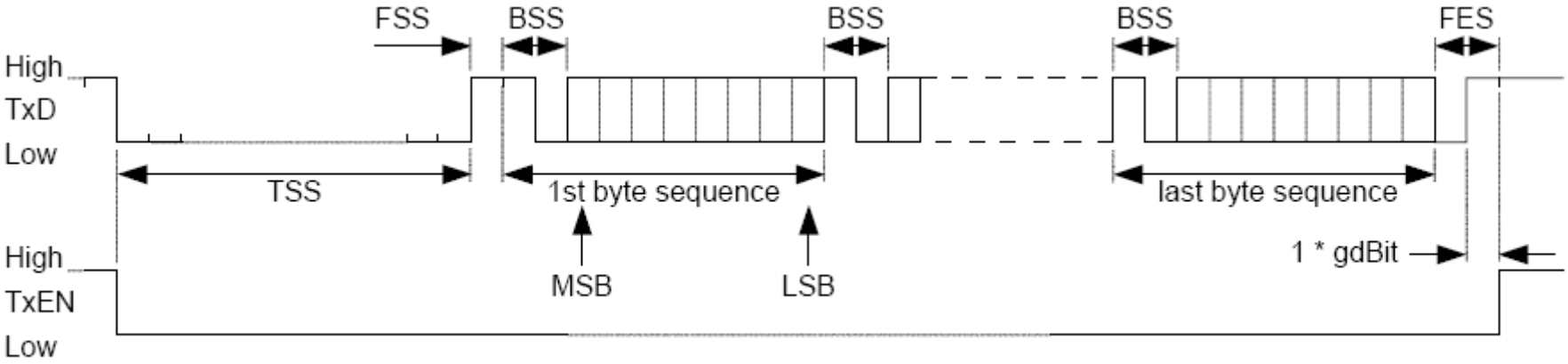
Frame format



- Reserved bit: for further protocol development
- Payload preamble indicator
  - Presence of a network management vector
  - In the dynamic segment presence of a message ID
- Null frame indicator
  - If set to zero payload contains no valid data
    - All bytes in the payload section are set to zero
- Sync frame indicator
  - receiving nodes shall consider the frame for synchronization

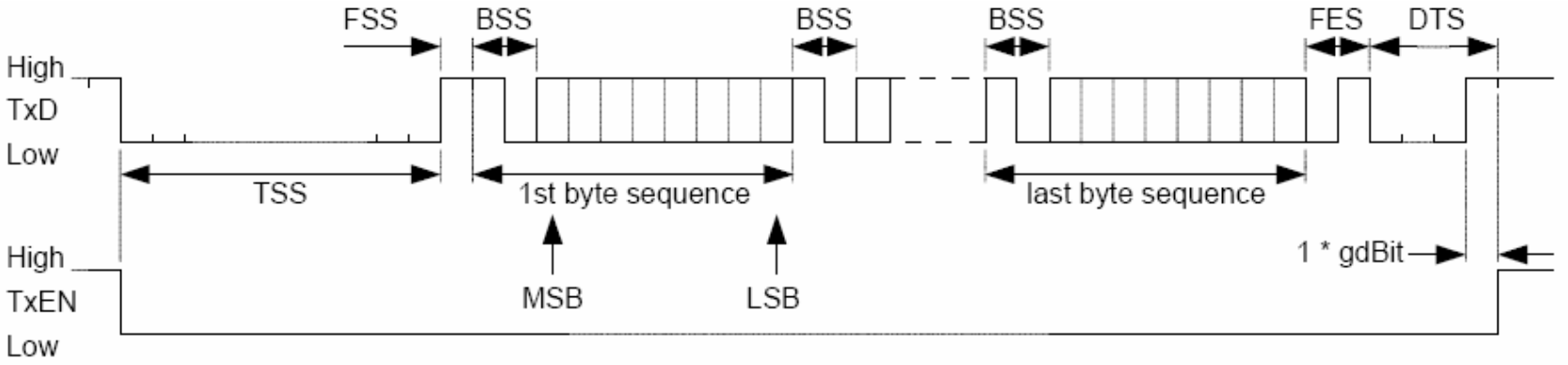
- Startup frame
  - Coldstart node allowed to send it to start other nodes
- Frame ID
  - defines the slot in which the frame should be transmitted
- Cycle count
  - the transmitting node's view of the value of the cycle counter

Frame encoding, static segment



- TSS: transmission start sequence
  - Low for a period given by a parameter
- FSS: frame start sequence
  - compensate for a possible quantization error in the first byte start sequence
- BSS: byte start sequence
  - bit stream timing information to the receiving devices
- FES: frame end sequence

Frame encoding, dynamic segment

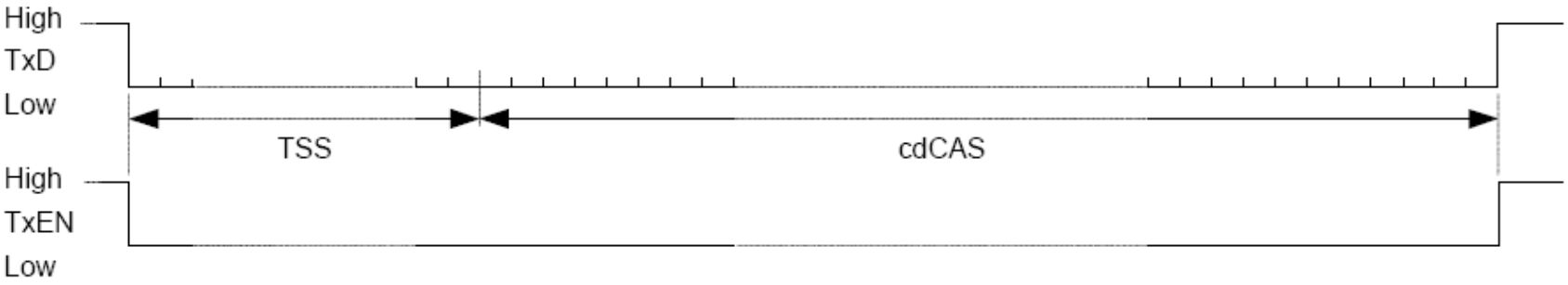


- DTS: dynamic training sequence
  - indicate the exact point in time of the transmitter's minislot action point
  - prevents premature channel idle detection by the receivers
- TxEN=High; low and idle different level

Frame bitstream assembly

- Break the frame data down into individual bytes.
- Prepend a TSS at the start of the bit stream.
- Add an FSS at the end of the TSS.
- Create extended byte sequences for each frame data byte by adding a BSS before the bits of the byte.
- Assemble a continuous bit stream for the frame data by concatenating the extended byte sequences in the same order as the frame data bytes.
- Calculate the bytes of the frame CRC, create extended byte sequences for these bytes, and concatenate them to form a bit stream for the frame CRC.
- 7. Append an FES at the end of the bit stream.
- 8. Append a DTS after the FES (dynamic segment).

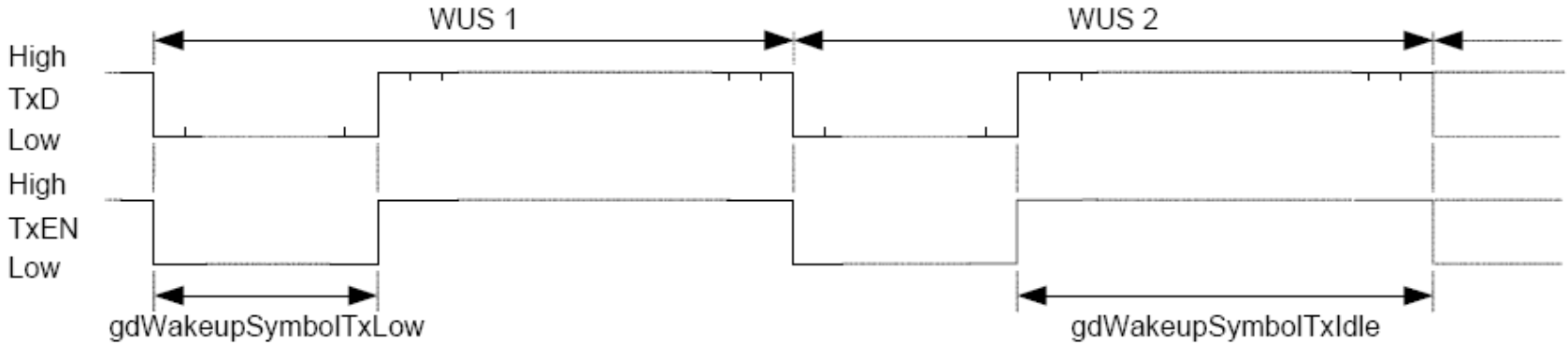
Symbol encoding



– CAS: collision avoidance symbol

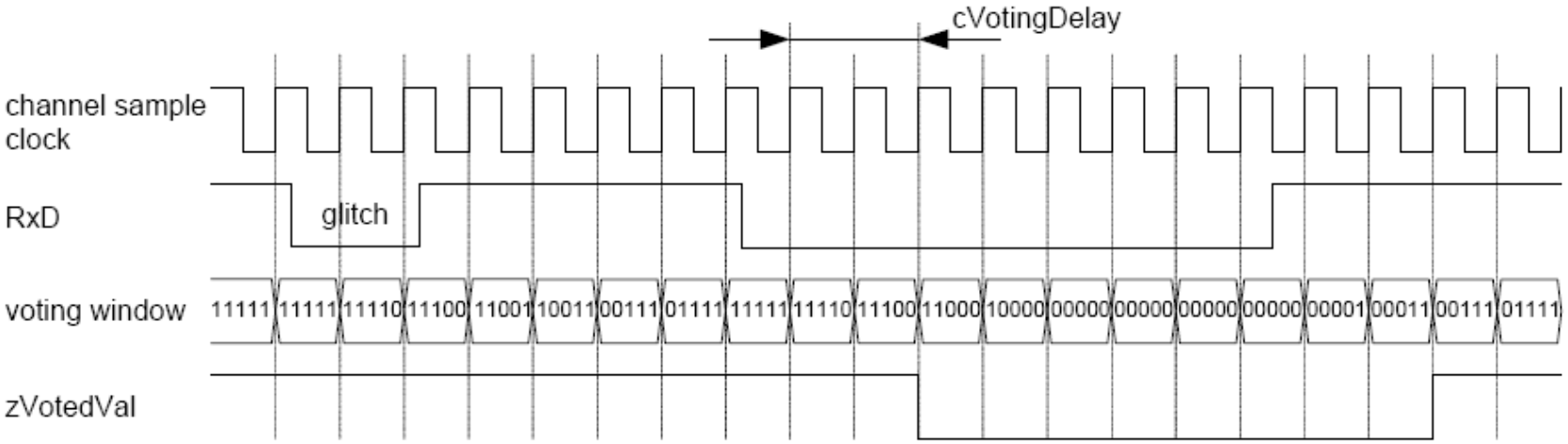
– MTS: media access test symbol

- Same encoding



Wake up symbol Idles

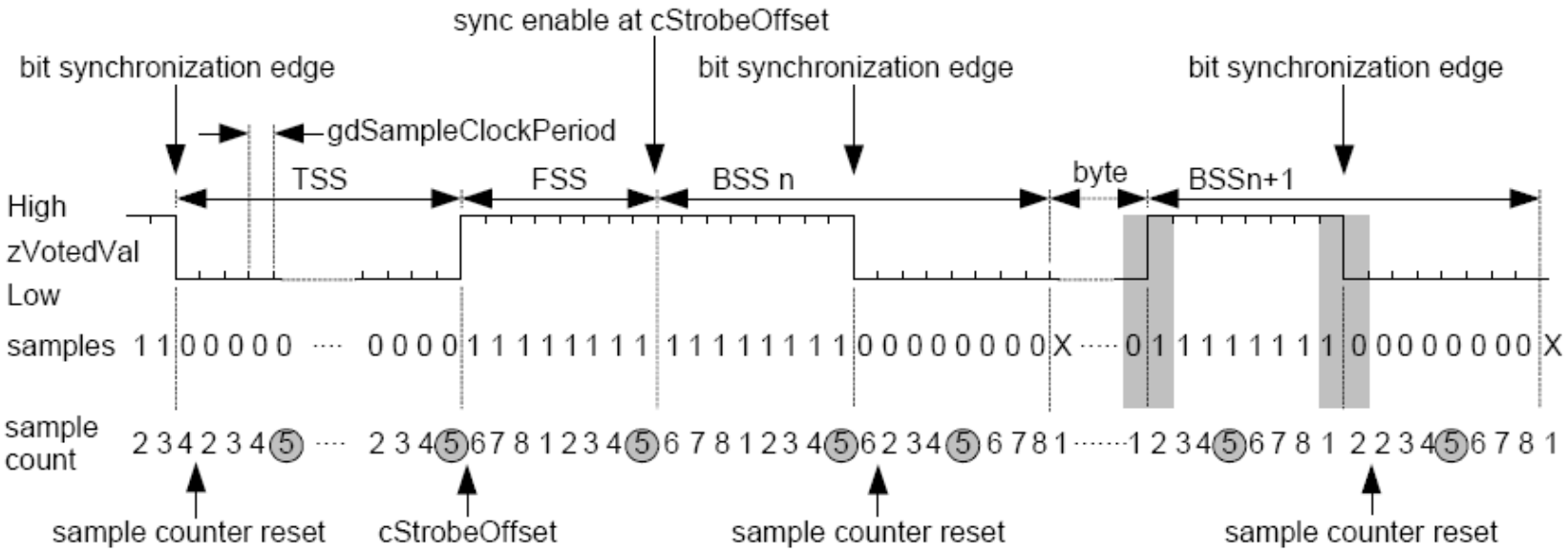
Sampling and majority voting



- Node shall perform sampling on RxD input
- The majority voting mechanism is a filter for suppressing glitches (spikes) on RxD input
- Receive node accept the voted value of bit in the middle of the bit time

Bit synchronization

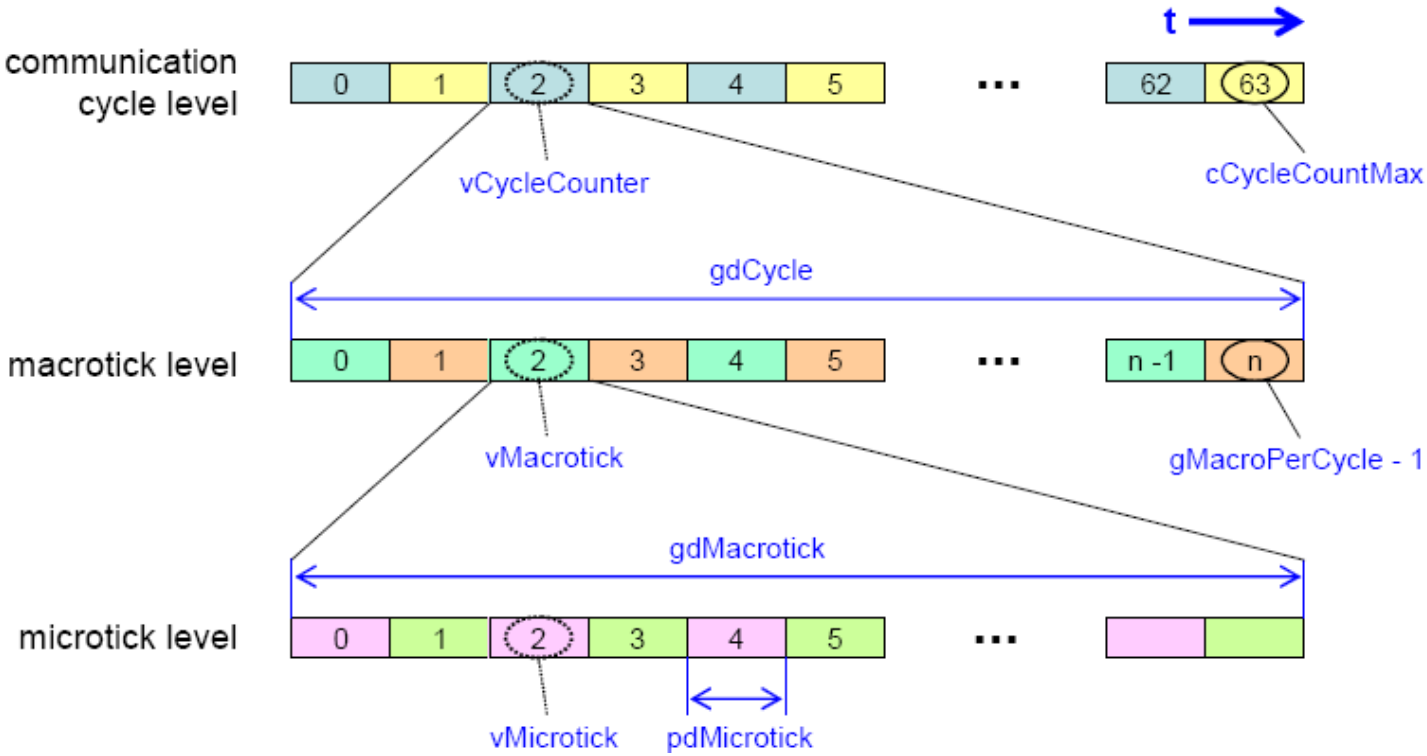
- Receive node counts the samples within bit time
- Synch is only performed when it is enabled



Clock synchronization

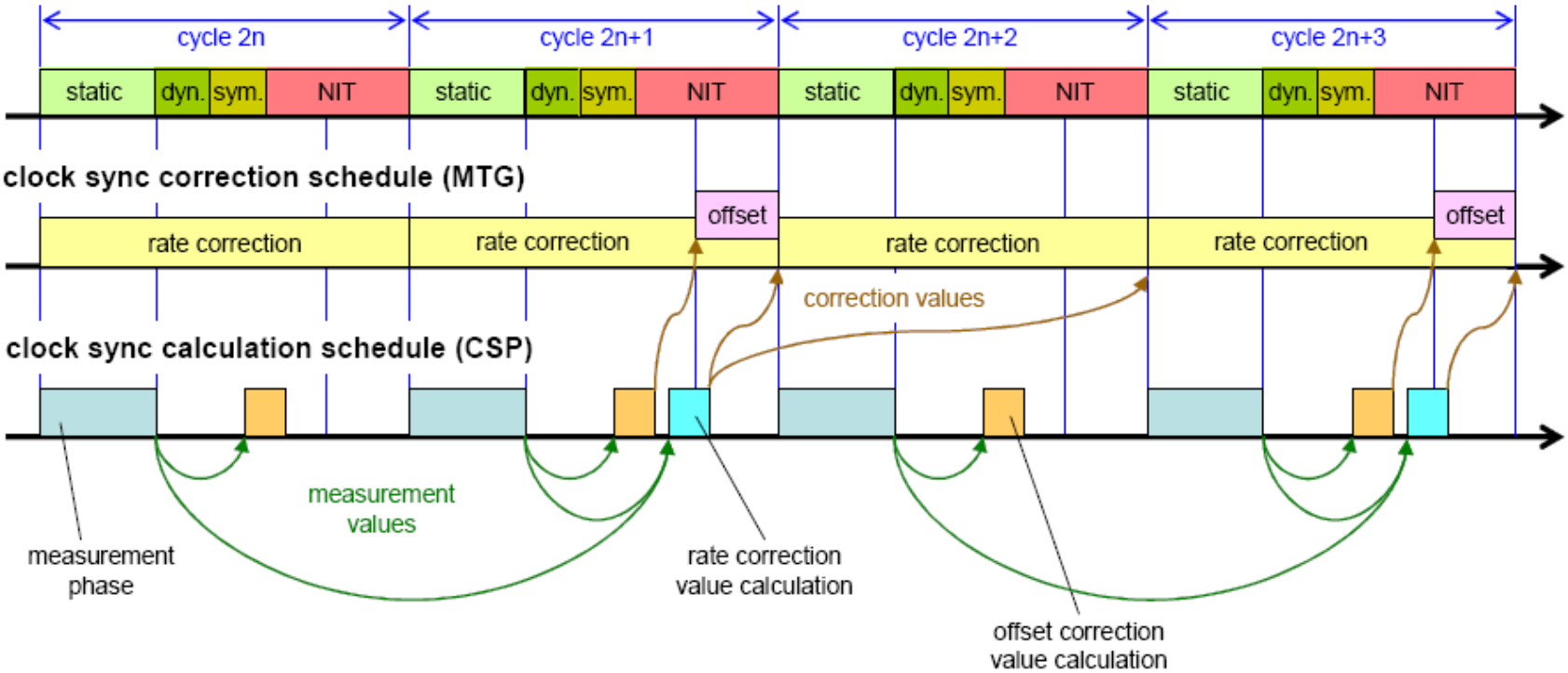
- Every node has its own clock
- Assumptions
  - In the system each node has approximately the same clock stability
  - Clock deviation cannot exceed a value
- Distributed clock signal

Timing hiearchy



- Microticks are controller-specific units
- Macroticks are synchronized on a cluster-wide basis

Synchronization process



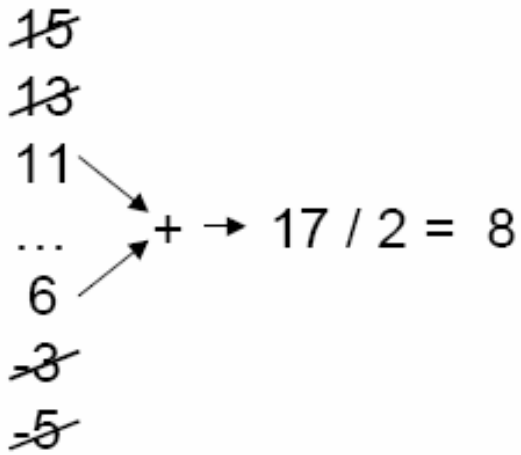
- Clock offset and rate correction
- Measurement: each node measures the difference of edge of expected and real sync frame in microtic

Offset correction

- Measurement
- Assignment of time deviation
- If no sync frame -> error
- Fault-tolerant midpoint calculation
- Inside the limit? If no -> crop
- External correction is also possible (from host)

- Fault-tolerant midpoint calculation

Number of values	k
1 - 2	0
3 - 7	1
> 7	2



  - Determination of value ‘k’
  - Dropping out ‘k’ pieces of highest and lowest values
  - Calculating the average coerced towards 0

Rate correction

- Measurement the time deviation of two consequtive cycles
- Use a table, see last N time periot
- If no sync frame -> error
- Fault-tolerant midpoint calculation
- Damping value decides the necessity of correction
- Inside the limit? If no -> crop
- External correction is also possible (from host)

External clock synchronization

- Even if nodes are synch-ed inside a cluster, the clusters can have sync error
- Host defined rate and offset correction for clusters
- Clock correction: setting the number of microticks inside macroticks

Wake-up

- Every bus driver should have power supply
- If wake-up symbol is detected by bus driver comm. controller is started (no ack)
- Different cotrollers for channel A and B
  - In case of coldstart node: if dual channel wake-up is detected on one channle wake-up signal sent to the other also

Start-up

- Goal: maintain sync-ed state of nodes inside a cluster in TDMA-based comm
  - The whole cluster be woken-up
  - Start-up on each channel at the same time
  - Start-up initiated by only a coldstart node
- Coldstart
  - Collision avoidance symbol (CAS)
  - only this node can transmit in the first 4 cycles
  - Integration: first other coldstart nodes + non coldstart nodes

- Number of coldstart nodes:
  - 3 if number of nodes >=3
  - 2 if number of nodes <2
- Start-up frame is a sync frame->colstart node is a sync node
- At least 2 error-free coldstart->cluster start

References

- FlexRay Communications System Electrical Physical Layer Specification Version 2.1 Revision B
- FlexRay Communications System Protocol Specification Version 2.1 Revision A