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| |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Isolator vs. Optocoupler Technology**  **1.0. Introduction**  Optocouplers have been the unchallenged signal isolation solution for over 40 years, but digital isolators fabricated in complementary metallic oxide semiconductor (CMOS) process technology are gaining favor in the design community because of their superior performance, reliability and integration. This paper explains the underlying technologies of digital optocouplers and [digital CMOS isolators](http://www.silabs.com/products/power/isolators/Pages/default.aspx) with side-by-side comparisons of performance and reliability.  **Table of Contents**   * [Digital Optocouplers and CMOS Digital Isolator Basics](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#2) * [Device Performance](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#3) * [Device Reliability](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#4) * [Common Mode Transient Immunity (CMTI)](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#5) * [Electromagnetic Interference (EMI)](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#6) * [Ease of Use](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#7) * [Optocoupler Replacement Upgrades](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#8) * [Summary](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#summary)     **2.0. Digital Optocouplers and CMOS Digital Isolator Basics**  Digital optocouplers are available in several versions from 4-pin devices costing pennies to expensive high-speed devices. The most popular, moderate-cost optocouplers are typically 8-pin LED-based devices that require an output side bias voltage and use input-side current to control the output state. Referring to Figure 1A, most optocouplers are composed of a light-emitting diode (LED), photo detector and output driver (usually a transistor or buffer). Current flowing though the LED causes emitted light to strike the photo detector, causing current flow from VDD to the base of the output device driving the output low. Conversely, the absence of LED current inhibits current flow to the output device, resulting in output logic high. Figure 1B is a top-level block diagram of a CMOS digital isolator, where a high logic level input enables a high-frequency carrier to propagate across the isolation barrier to create a logic high level at VOUT.  **Basic Operation of Optocoupler vs. CMOS Digital Isolator**   |  |  |  | | --- | --- | --- | | Optocoupler |  | CMOS Digital Isolator | | **Figure 1A. Optocoupler** |  | **Figure 1B. CMOS Digital Isolator** | | Optocoupler X-Ray |  | Digital Isolator | | **Figure 2A. Optocoupler Package X-Ray** |  | **Figure 2B. Decapsulated 6-Channel CMOS Digital Isolator** |   Figure 2A shows an X-Ray view of a single-channel optocoupler where the LED and photo coupler die are attached to a split lead frame and separated by a physical gap (distance through insulation [DTI] 80 µm to 1,000 µm gap between the LED and optical receiver die) and transparent insulating shield. More recent optocoupler packaging also includes the addition of silicone filler (Figure 3). Optocouplers are fabricated in gallium-arsenide (GaAs) process technologies that are notorious for wide parametric variation over temperature, high input current, relatively low time-dependent device breakdown (TDDB) and intrinsic wear-out mechanisms.  Cross Sectional View of an Optocoupler  **Figure 3. Cross Sectional View of an Optocoupler**  The basic operating principal of the CMOS digital isolator is somewhat analogous to that of an optocoupler, with the exception that output logic state control is determined by the presence or absence of a high-frequency (HF) carrier instead of light as in the optocoupler. Figure 2B shows the die configuration and bonding of a 150 Mbps, six-channel CMOS digital isolator. The base isolator die is designed and fabricated such that wire-bonding two identical die together (Figure 2B) forms a transmitter and receiver separated by a differential capacitive isolation barrier. The isolator output state is determined by either an input logic level or an input current (similar to the optocoupler), depending on the part number.  The heart of any digital isolator is the isolation barrier that safely withstands the applied high-voltage stress. The optocoupler isolation barrier relies on a combination of a physical gap (i.e. distance through insulator or “DTI”), polyimide tape, silicon filler and plastic mold compound for insulation (Figure 3). This hybrid methodology not only makes increased optocoupler integration difficult, but it increases fabrication complexity and therefore cost and reliability. That being said, the many members of the International Standards community still specify isolation barrier requirements based on optocoupler DTI. Fortunately, the standards agencies tests are based on barrier withstand voltage, regardless of device implementation. Please see section 4.0 in this document for a discussion of insulation materials and their effects on isolation performance.  CMOS construction and careful attention to design enable CMOS digital isolators to achieve higher degrees of performance, reliability and ease-of-use, primarily thanks to these key enabling technologies:   * **Mainstream, low-power CMOS process technology instead of GaAs:** CMOS is the highest performance, most reliable and most cost-effective process technology available. Devices fabricated in CMOS exhibit superior timing, integration, operating stability and reliability characteristics compared to gallium arsenide processes. * **High frequency carrier modulation instead of light:**The combination of the precision, high-frequency carrier and narrow receiver passband provides tight frequency discrimination for outstanding noise rejection and, therefore, higher data integrity. * **Fully differential isolation path instead of single-ended:** Optocouplers are single-ended devices and are subject to CMT perturbations, whereas the differential signal path and high receiver selectivity of CMOS digital isolators provide high rejection of common-mode transients up to 50 kV/µS, external RF field immunity as high as 300V/m and magnetic field immunity beyond 1000 A/m. * **Proprietary EMI design techniques:** CMOS digital isolators meet the FCC Part B emission standards for conducted and radiated EMI. For more information on CMOS isolator emissions, susceptibility and reliability vs. optocouplers, see Silicon Labs' white paper “CMOS Isolators Supersede Optocouplers in Industrial Applications” available at [www.silabs.com/isolation](http://www.silabs.com/isolation).   **2.1. Isolator Requirements:** Isolator parametric requirements are dictated by the needs of the end application, and designers tend to stress the importance of certain isolator parameters over others. For example, isolators operating in a noisy industrial environment might cause a designer to prioritize high common-mode transient immunity (CMTI) over low-power operation, whereas a high-precision ADC application might cause the designer to prioritize low jitter over pulse width distortion, and so on. In short, many applications will care most about just a few key isolator parameters, and designers will often verify these parameters independently to ensure they meet the system requirements. The more common isolator parameters and their definitions are shown in Table 1 for reference. | |
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Typical Isolator Parameters and Definitions**   |  |  |  | | --- | --- | --- | | **Isolator Parameter** | **Symbol** | **Definition** | | **Channel-to-Channel Skew** | tPSK | The propagation delay time difference between channels in a multichannel isolator | | **Common Mode Transient Immunity** | CMTI | The ability of an isolator to reject fast common-mode transients | | **Device Start-up Time** | tSU | The time delay from power-on to proper isolator operation. | | **Input High, Low Thresholds** | VIH, VIL | Voltage threshold value that must be crossed to achieve input high or low levels | | **Input Leakage Current** | IL | Parasitic leakage current flowing into an input-side pin | | **Input-Side Bias Current** | IDDI | Current that provides bias current to the isolator input-side circuits | | **Jitter** | tJIT(pk) | Variation of the pulse edge position of the data stream | | **Undervoltage Lockout** | UVLO | The VDD bias level required to enable or disable isolator operation | | **Maximum Data Rate** | Dmax | Highest isolator data rate (usually specified in Mbps) | | **Minimum Pulse Width** | t(min) | The minimum width pulse that can be recognized by the isolator | | **Output Impedance** | Zout | The characteristic output impedance (typically measured in Ω) | | **Output Rise, Fall Times** | tr, tf | The time period for an output edge to rise from 10% to 90% of VDD or fall from 90% to 10% of VDD) | | **Output Voltage High, Low** | VOH, VOL | The output threshold levels that define a logic 1 and logic 0 | | **Output-Side Bias Current** | IDD | Bias current flowing into the isolator output-side | | **Propagation Delay** | tPHL, tPLH | The time period required for an isolator input event to propagate to the isolator output | | **Propagation Delay Skew** | tPSK (p-p) | The difference between the min and max propagation delays (tPLH or tPHL) for any given group of isolators operating under the same conditions | | **Pulse Width Distortion** | PWD | The difference between high-to-low and low-to-high propagation delay (tPLH – tPHL) |   [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top)  **3.0. Device Performance**  This section compares the performance of CMOS digital isolators (most notably the Si86xx series) against competing optocouplers, such as the HCPL-4506, HCPL-2400 and others. Note that all Silicon Labs isolators (i.e. the Si84xx, Si86xx, Si87xx series) are based on Si86xx technology and, therefore, have substantially the same performance and reliability. While Table 1 lists many key isolator parameters, designers appreciate isolators that have attributes like those listed below:   1. **Well-defined, key operating parameters that exhibit little change over voltage, temperature and device age.** Isolators vulnerable to significant changes in temperature, current and/or device age force the designer to give-up design margin, reducing system performance. This is especially true in isolated high-speed data systems that rely on tight timing relationships. 2. **High reliability** Isolator lifetimes of 20+ years are now required by applications, such as HEV/EV, solar and wind energy systems and, typically, operate in elevated temperature environments over 120 °C. 3. **High CMTI** Noisy industrial environments require robust isolation devices that have high immunity to common mode transient events to ensure data integrity. 4. **Minimal electromagnetic interference (EMI) and high external electrical and magnetic field immunity** EMI is a source of potential data corruption, especially in medical applications that acquire low-amplitude signals, such as electrocardiographs (ECG). External magnetic and electric fields can degrade system performance, so the ability of an isolation device to reject external field interference is critical. 5. **Ease of Use** The best isolation devices are well documented, predictable, reliable, and intuitively easy to apply. These points are covered in detail in the paragraphs below.   **3.1. Timing Variation with Temperature:** Figure 4 compares propagation time and pulse width distortion stability over temperature for the HCPL-2400 20 Mbps digital optocoupler and the Si8660Bx 10 Mbps CMOS digital isolator. Referring to Figure 4A, the HCPL-2400 data sheet curve shows that the propagation delays, tPHL and tPLH, are not matched, so additional system design margin may be required to ensure that the slower of the two propagation times is met (depending on the user’s timing requirements). The propagation delays remain uniform at a worst-case value of 33 ns between -40 °C and +35 °C but slow to 40 ns at 70 °C (and potentially increase with elevated temperature as indicated by the dashed lines). The blue curves at the bottom of Figure 4A show the propagation delay time of the Si8660Bx over the temperature range, from -40 °C to +125 °C. Note that tPHL and tPLH are symmetrical and faster than the propagation times of the HCPL-2400. The HCPL-2400 PWD data sheet curve (Figure 4B) is similar to that of Figure 4A, suggesting the same underlying thermal sensitivity; PWD remains flat at 3 ns over the temperature range of -40 °C to +38 °C but worsens to 6 ns at 69 °C. The Si8660Bx curve at the bottom of Figure 4B shows a considerably lower PWD over the temperature range of -40 °C to +125 °C with a deviation of 3 ns at the graph’s limit (69 °C) and 4.5 ns at +125 °C.  Si8660Bx Isolators Propagation Delay and PWD over Temperature  **Figure 4. HCPL-2400 and Si8660Bx Isolators Propagation Delay and PWD over Temperature**  Figure 5 shows the effect of the HCPL-2400 optocoupler input current on propagation delay time as documented in the manufacturer’s application note. The optocoupler was tested with and without a “peaking” capacitor (Cp), which momentarily increases LED current during turn-on and turn-off for improved response. Again, tPHL and tPLH are not symmetrical and, therefore, must be examined individually. The optocoupler of curve A is subjected to an input current of 0.5 to 1.0 mA with peaking capacitor Cp = 20 pF. The combination of elevated input current and faster turn-on and turn-off due to Cp results in a flatter response and shorter propagation time relative to that of the other curves. The blue curve at the bottom of the chart shows the propagation time of the CMOS digital isolator, which exhibits a flatter symmetrical curve over the temperature range from -40 °C to  +125 °C.  Optocoupler vs. CMOS Isolator Propagation Delay  **Figure 5. Optocoupler vs. CMOS Isolator Propagation Delay**  While these examples demonstrate the changes in propagation time and pulse width distortion, other optocoupler parameters can wander with temperature, device age and other influences, such as optocoupler current transfer ratio, threshold settings, and output impedance, mostly caused by behaviors related to LED emission and the underlying GaAs process technology.  Section Summary: Optocouplers suffer from asymmetric propagation delays and large parametric deviation with temperature, both of which are related to the underlying GaAs process technology. These issues cause designers to compensate by sacrificing design margin, potentially reducing system performance. In contrast, CMOS digital isolators exhibit symmetrical delays and little parametric deviation over an operating temperature range much wider than that of optocouplers.  [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top)  **4.0. Device Reliability**  This section summarizes the isolation-related specifications in the data sheet, distinguishes between long term and short term ratings, provides a simple tool to compare products from different manufacturers and explains why the SiO2-based insulation barrier from Silicon Labs delivers the best performance from an isolation perspective.  All isolation devices, optocouplers or CMOS isolators, have voltage withstand specifications listed in the data sheet. For example, the table below is from the data sheet for the HCPL-4502, an open-collector Avago optocoupler. | |
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Data Sheet Ratings for the HCPL-4502**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Description** | **Symbol** | **Characteristic  HCPL-4502/4503** | **Characteristic  HCPL-0452/0453** | **Units** | | Maximum Working Insulation Voltage | VIORM | 630 | 560 | Vpeak | | Input to Output Test Voltage, Method b\* VIORM X 1.875 = VPR, 100%  Production Test with tm = 1 sec, Partial Discharge < 5 pC | VPR | 1181 | 1050 | Vpeak | | Input to Output Test Voltage, Method a\* VIORM X 1.5 = VPR,  Type and sample Test, tm = 60 sec, Partial Discharge < 5 pC | VPR | 945 | 840 | Vpeak | | Highest Allowable Overvoltage\* (Transient Overvoltage, tini = 10 sec) | VIOTM | 6000 | 4000 | Vpeak |   Of these ratings, only the Maximum Working Insulation Voltage (VIORM) implies a guarantee over time. All other specifications are only valid for time zero. In other words, these specifications are not guaranteed over the lifetime of the product, but only for a single instance of short-term (typically 1 second or 1 minute) voltage stress. Isolation devices are comprised of a dielectric insulation barrier that provides the voltage withstand capability. All dielectrics exhibit aging; this implies a lifetime for which the voltage-withstand specification is valid.  Aging is primarily due to dielectric degradation from thermal and/or electric energy fields. For a particular dielectric, this is determined by its intrinsic material and manufacturing properties (impurities, defects etc.). Aging is a non-reversible process, and, at the point of dielectric fatigue or failure, an avalanche current flows through the dielectric, causing it permanent damage. A high-voltage isolation lifetime implies that, at the end of this time period, its dielectric properties can no longer be guaranteed.  Depending on the dielectric material used to construct the insulation barrier, the resulting isolation device could have very different properties. Silicon Labs uses silicon dioxide (SiO2) for insulation because it is the most commonly used dielectric in the semiconductor industry. This is due to the processing technology having matured to the point where defect levels in SiO2 are among the lowest of all dielectrics and can guarantee long product service lifetimes. SiO2 is also one of the highest quality dielectrics available and has a breakdown threshold of 1000 V/µm compared to ~50 V/µm for the mold compound used for insulation by optocouplers. In addition, SiO2 is one of the most stable dielectrics over variations in temperature and moisture and is an inorganic material as opposed to mold compound, which is organic. This means that with SiO2 as the insulation, Silicon Labs isolation products offer Industry-leading withstand properties compared to optocouplers.  All isolation product manufacturers provide this lifetime information, at the expiration of which, the devices are no longer guaranteed to function as isolators. In all cases, the failure mode is a resistive short between the two (once isolated) grounds of the isolation device - a short from the input to the output side. This failure mechanism is independent of the coupling technique and applies to all isolators; it is a fundamental dielectric property. As an example, refer to the high-voltage lifetime reports from manufacturers below: Avago: app note AN 1074, Texas Instruments app note SLLA 197.  For measuring high-voltage dielectric lifetimes, it is important to understand how dielectric aging is physically explained and characterized by various models like the E-model, 1/E model, a combination of the two or other lesser-known models. The E-model is the most conservative, and its mathematical statement is given below. It states that the time to failure (TF) has an inverse exponential relationship to the applied electric (E) field.  E-model: ln(TF) = (ΔHo/Kb\*T) – Ψ\*E, where  TF is the time to fail  ΔHo is the enthalpy for dielectric breakdown (also referred to as activation energy which depends on the dielectric materials used and the process technology)  Kb is Boltzmann’s constant  T is the temperature  E is the electric field across the isolation barrier, given by the ratio of applied stress voltage (Vrms) to thickness of the insulation barrier  Ψ is the field acceleration parameter. This depends on the dielectric material properties as well.  Time Dependent Dielectric Breakdown (TDDB) methodology is used to estimate the continuous operating voltage of an isolator. It starts by measuring the time to fail for given devices under highly accelerated voltages; this data is then extrapolated to the working voltage or continuous rated voltage for the product to determine its lifetime. In the methodology used by Silicon Labs to characterize the dielectric using E-model, the temperature is a constant (worst case Tj of 150 °C was used) and the insulation barrier thickness is a constant for a given product, hence, the equation reduces to:  TF = exp(-B\*V) where B is a constant for a given product/device under test and V is the applied voltage.  When plotted on a log-normal graph as below, the exponential relationship expected in the E-model is mathematically represented by a straight line.  *Note: Not all isolator manufacturers use the E-model. Our decision to use the E-model is based on the fact that it is the most widely accepted model and the most conservative.*  Standard TDDB methodology was used to calculate lifetime expectancy. Breakdown tests were run at various voltages. Results were then plotted on a Weibull distribution to extrapolate the raw data to 10 ppm fail rates. This implies that at the stated time to fail values, only 10ppm of the devices under test would have failed. This is an extremely low failure rate, thus the lifetimes stated are very conservative. These 10 ppm values were used to plot the TDDB graph of time to fail (TTF) vs. voltage as shown in Figure 6 below. The mean time to fail (MTTF) is also plotted in the TDDB graph below.  TDDB graph of time to fail vs. voltage  **Figure 6. TDDB graph of time to fail vs. voltage (10 ppm and mean)**  Based on the above chart, the results for various working voltages are summarized for convenience in Table 3 below. At a working voltage of 800 Vrms, the 10 ppm time to fail is 265 years, while at 1200 Vrms working voltage, life expectancy is 53 years. This is the best high-voltage lifetime rating of any isolator available today.  One concern that customers have is whether the product has been tested at voltages much closer to the working voltages as a litmus test for TDDB extrapolation. To address that concern, Silicon Labs has started a test at 1600 Vrms. As of the writing of this report, there have been no fails with more than 1000 hours logged on the test. | |
| |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Table 3. MTTF Results of High Voltage Lifetime Study**   |  |  |  |  | | --- | --- | --- | --- | | **Si86xx Applied Voltage** | | **10 ppm Time To Fail, years** | **Mean Time To Fail, years** | | **Vrms** | **Vpeak or V** | | 800 | 1120 | 265 | 2367 | | 1200 | 1680 | 53 | 478 | | 1600 | 2240 | 10 | 96 |   Optocoupler manufacturers have also conducted similar studies to rate their products. The chart below is from app note AN-1074 on [www.avagotech.com](http://www.avagotech.com/). No TDDB model is mentioned, only a safe operating area is defined as shown in the Figure 7 below. According to the chart, only voltages less than 800 V continuous even have a lifetime rating. At 1600 V, safe lifetime is only 200 hours. The Silicon Labs product lifetime for 1600 V is 10 years.  Avago High Voltage Lifetime Rating for Optocouplers  **Figure 7. Avago High Voltage Lifetime Rating for Optocouplers**  In summary, Silicon Labs isolators provide robust isolation that matches the time zero data sheet specifications of optocouplers and outlasts optocoupler lifetimes by an order of magnitude or more.  [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top) | |
| |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **5.0. Common Mode Transient Immunity (CMTI)**  Common mode transient immunity (CMTI) refers to the ability of the isolator to reject fast common-mode transients and is typically measured in kV/µs. Common mode transients are one of the leading causes of data corruption in isolation applications. CMTI is important because high slew rate (high-frequency) transients can couple through parasitic capacitance across the isolation barrier, corrupting data. The schematic diagram for the CMTI test setup and test board photo used in this paper appear in Figure 8, while Figure 9 shows the dominant parasitic couplings within the HCPL-4506 optocoupler.  CMTI Test Schematic and Test Board Photo  **Figure 8. CMTI Test Schematic and Test Board Photo**  Referring to Figure 9, the single largest parasitic coupling is CLEDN, which is effectively short-circuited across the impedance of VCM when the optocoupler is configured in grounded cathode mode as shown. That said, the remaining parasitic couplings, while somewhat weaker, remain capable of creating CMT-induced data errors. The Si8712A is an optocoupler upgrade that directly replaces commodity optocouplers without changes to the PCB and provides substantially better performance, reliability and power efficiency (note the Si8712A is the low-power, low CMTI Si87xx product version).  Device testing was performed with an external pull-up resistor instead an internal pull-up resistor because the parasitic coupling of CLED02 is weaker than that of CLED01. The stronger parasitic coupling of CLED01 combined with the high 20K Ω internal pull-up resistor would increase the probability of data errors due to CMT events for the optocoupler and, to a much smaller extent, the Si8712A. The test results shown in Figures 9 through 13 compare side-by-side the CMTI performance of the Si8712A CMOS digital isolator to that of the HCPL-4506 optocoupler. While both isolation devices are configured identically per Figure 8, the Si8712A the internal parasitic couplings of the Si8712A are 2 to 3 times lower than those of the optocoupler, enabling higher CMTI performance.  Optocoupler Internal Parasitic Couplings  **Figure 9. HCPL-4506 Optocoupler Internal Parasitic Couplings**     |  |  |  | | --- | --- | --- | | Positive CMTI Response for CMOS Isolator Si8712A |  | Positive CMTI Response for HCPL-4506 Optocoupler | | **Figure 10A. Positive CMTI Response for CMOS Isolator Si8712A** |  | **Figure 10B. Positive CMTI Response for HCPL-4506 Optocoupler** |   Figure 10 applies logic high to the anode pin of both devices, causing the output of both devices to remain low. The top trace of Figure 10A shows a positive-going 1.5 kV CMT pulse, while the bottom trace shows the effects of the internal coupling to collector pull-up resistor. As shown, the amplitude of this disturbance is on the order of 100 mV for the Si8712A compared to 500 mV for the optocoupler (Figure 10B).  The test of Figure 11 applies logic zero to the input of both devices, causing the output of both devices to remain high. Again, the top trace shows the negative-going CMTI pulse. Figure 11A shows the output of the Si8712A dipping negative to -250 mV(pk) compared to -1.1 V(pk) for the optocoupler (Figure 11B). Note that the Si8712A exhibits both lower amplitude and faster recovery time. The CMT event of Figure 12 increases fall time to 200 ns, which has the effect of reducing CMT amplitude, but increasing recovery time.   |  |  |  | | --- | --- | --- | | Negative CMTI Response for CMOS Isolator Si8712A |  | Negative CMTI Response for HCPL-4506 Optocoupler | | **Figure 11A. Negative CMTI Response for CMOS Isolator Si8712A** |  | **Figure 11B. Negative CMTI Response for HCPL-4506 Optocoupler** |      |  |  |  | | --- | --- | --- | | Negative CMTI Response for CMOS Isolator Si8712A |  | Negative CMTI Response for HCPL-4506 Optocoupler | | **Figure 12A. Negative CMTI Response for CMOS Isolator Si8712A** |  | **Figure 12B. Negative CMTI Response for HCPL-4506 Optocoupler** |   While the above tests show the effect of singular parasitic events, multiple couplings can combine to create unwanted effects as shown in Figures 12A through 13D. Referring to Figure 12A, the optocoupler input is maintained logic high (output low), and, this time, the internal 20 kΩ pull-up resistor is used. The LED cathode is exposed to a 40 ns CMT rise time, which rapidly level-shifts the LED cathode and anode voltages, causing parasitic current to be injected through CLED02 to the Vo pin while, at the same time, CLED01 diverts current from IF into the RL pin. This “1-2” combination causes the current in both the LED and the internal pull-up resistor to be reduced at the same time,   |  |  |  | | --- | --- | --- | | Internal Parasitic Coupling within the HCPL-4506 Optocoupler |  | Internal Parasitic Coupling within the HCPL-4506 Optocoupler | | **Figure 13A. Internal Parasitic Coupling within the HCPL-4506 Optocoupler** |  | **Figure 13B. Internal Parasitic Coupling within the HCPL-4506 Optocoupler** | | Internal Parasitic Coupling within the HCPL-4506 Optocoupler |  | Internal Parasitic Coupling within the HCPL-4506 Optocoupler | | **Figure 13C. Internal Parasitic Coupling within the HCPL-4506 Optocoupler** |  | **Figure 13D. Internal Parasitic Coupling within the HCPL-4506 Optocoupler** |   further reinforcing the momentary output turn-off, as evidenced by the 1 V(pk) glitch of Figure 13A. Note also the LED parasitic turn-on is delayed due to the long propagation time of the optocoupler. Figure 13B shows the same test as Figure 13A, with the exception of the CMT rise time increasing to 80 ns, which has the effect of reducing the internal pull-up coupling but increasing the amplitude of the LED parasitic turn-on. This trend continues in the 120 ns CMT pulse of Figure 13C and is especially pronounced in Figure 13D, where the internal pull-up coupling is virtually gone, but the parasitic turn-on pulse amplitude is several volts.  Section Summary: The optocoupler’s inherently high internal parasitic coupling and parasitic interdependencies (as shown in Figures 9 and 13) can individually or collectively create false positives and negatives of various durations and amplitudes, corrupting data transmission and reducing overall system performance. This issue is compounded by the notoriously poor CMTI characteristics of optocouplers.  [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top) | |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **6.0. Electromagnetic Interference (EMI)**  EMI refers to any electromagnetic disturbance that disrupts or otherwise interferes with the effective performance of authorized electrical equipment. As it pertains to isolators, radiated and conducted EMI is generally the product of high frequency switching circuits (and their harmonics) that couple into other circuits and/or the environment. Radiated EMI is analogous to broadcast in that it travels from transmitter to receiver through free space, whereas conducted EMI travels along a conductor. The FCC sets limits for both conducted and radiated EMI, and all devices in a given class must comply.  Specifications published by various certification agencies place limits on conducted and radiated EMI; one of the more common specifications is FCC Part 15, which covers circuit assemblies used in or near the home. Testing to this specification is conducted in an open air environment using a 10 meter antenna positioned approximately 5 meters above the ground plane. Another specification, SAEJ1752-3, is more IC centric in its test methodology, and recommends mounting the IC to be tested on a small circuit board, then measuring the radiated emissions from the board while operating within the actual application environment.  EMI testing to FCC Class B Part 15 (Figure 14) was performed using two of the test boards, where each board contained a 6-channel CMOS digital isolator with all inputs tied high to maximize emissions from the internal transmitters. The EMI plots below show the total emissions from 12 channels switching at full speed on two boards (results summarized in Figures 14A-14D). This independently-conducted test showed the CMOS digital isolator passed FCC Class B Part 15, achieving low EMI operation primarily through a combination of the field-canceling internal differential signal path, the sizing of the isolation capacitors, and the design of the low-power main oscillator. (Note the low frequency noise of Figure 14A was caused by tester noise and not the CMOS digital isolator).  As for the optocoupler, here we see perhaps their only advantage - because the optocoupler uses light as its carrier, it is immune to external magnetic and electric field interference.  Si86xx EMI X-Axis with Input Logic 0  **Figure 14A. Si86xx EMI X-Axis with Input Logic 0**  Si86xx EMI Y-Axis with Input Logic 0  **Figure 14B. Si86xx EMI Y-Axis with Input Logic 0**  Si86xx EMI X-Axis with Input Logic 1  **Figure 14C. Si86xx EMI X-Axis with Input Logic 1**  Si86xx EMI Y-Axis Measurements Input Logic 1  **Figure 14D. Si86xx EMI Y-Axis Measurements Input Logic 1**  Section Summary: The optocoupler has perhaps the lowest EMI of all silicon-based isolators, with the exception of the Silicon Labs Si8xxx family. These CMOS digital isolators passed FCC Class B Part 15 and have industry-leading EMI performance.  **6.1 RF Immunity:** RF immunity refers to the ability of an isolator to reject strong local electromagnetic fields, thereby maintaining error-free data transfer. Intuitively, one would expect ambient RF fields to interfere with the CMOS digital isolator’s internal HF data transmission. However, a CMOS digital isolator demonstrates an extremely high degree of external RF immunity by virtue of its design. Local fields induce common-mode voltages within a CMOS digital isolator’s internal signal path that are rejected by a combination of the CMOS digital isolator’s differential isolation signal path and high receiver selectivity due to the tight matching of signal levels on each side of the internal differential signal path. This architecture causes common-mode voltages at the receiver differential inputs to be rejected. The receiver then *amplifies only the differential input voltage within a very narrow frequency band and rejects all other input.* Together, these mechanisms reject interference from a variety of external fields and enable very high CMTI and robust operation, even in electrically noisy environments.  CMOS Isolator E-Field Immunity  **Figure 15. CMOS Isolator E-Field Immunity**  The CMOS digital isolator can be used in close proximity to large motors and other magnetic field-producing equipment. It is theoretically possible that data transmission errors could occur if the magnetic field is far too large and/or far too close to the isolator. In actual use however, CMOS digital isolators provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/Meter (per IEC 61000-4-8 and IEC 61000-4-9). Such a field can be generated by pushing 107 amperes through a 0.1 m conductor located 0.1 m from the CMOS digital isolator. It is highly unlikely that such a condition would be found in any operating environment. Such a field will most likely destroy surrounding circuitry before damaging the CMOS digital isolator isolation barrier circuit.  Section Summary: While optocouplers provide the unique benefit of intrinsic external field immunity, the CMOS digital isolator exhibits virtually equivalent field rejection through its high receiver selectivity due to the tight matching of signal levels on each side of the internal differential signal path.  [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top)  **7.0. Ease of Use**  Large and interdependent parasitic couplings, temperature-dependent operating parameters and operating changes with device age make optocouplers challenging devices to apply. Conversely, CMOS digital isolators have substantially lower first order parasitics, fewer interdependent couplings and significantly better performance over operating temperature. Common optocoupler design issues are summarized here:  **7.1. Current Transfer Ratio:**Optocouplers have a temperature-dependent “gain term” called current transfer ratio (CTR). Typical CTR values will be between 10% and 50% for optocouplers with an output phototransistor and up to 2000% for optocouplers with a Darlington transistor output pair. Other CTR dependencies include output transistor current gain hfe, VDD supply voltage, forward current through the LED and ambient operating temperature. The value of CTR varies with absolute current level and peaks at an LED current level of about 10 mA, falling away at both higher and lower current levels.  Optocoupler CTR  **Figure 16. Optocoupler CTR**  **7.2. Digital Optocoupler Turn-on Thresholds:**Digital optocoupler turn-on and turn-off thresholds tend to be positioned at relatively low levels and are temperature sensitive as well; so, the actual threshold values can be rather nebulous from one unit to the next. Lab measurements have shown most optocouplers begin turn-on below the data sheet specified threshold, sometimes requiring additional external components for correction.  Si87xx Input Current Turn-on/Turn-off Thresholds vs. Optocoupler Thresholds  **Figure 17. Si87xx Input Current Turn-on/Turn-off Thresholds vs. Optocoupler Thresholds**  Figure 17 compares the Si8712A CMOS digital isolator thresholds to that of a typical digital optocoupler. As shown, the CMOS isolator is either on or off, which eliminates the need for a CTR specification and its related temperature sensitivities. The digital optocoupler has the diode characteristic of the internal LED, making consistent and precise turn-on/turn-off thresholds very difficult to implement.  **7.3. Added External BOM:** Optocouplers operating in electrically noisy environments commonly use additional components to increase CMTI performance, as shown in Figure 18. Input and output circuit modifications that help increase optocoupler performance include an external (instead of internal) pull-up resistors, reverse biasing or shorting the LED to ensure it remains in its correct state in the event of a CMT, and adding an external RC to filter out momentary output glitches, such as those shown in Figures 9 through 13 inclusive.  External Circuits for Optocoupler CMTI Improvement  **Figure 18. External Circuits for Optocoupler CMTI Improvement**  These optocoupler fixes should be made with care as some of them can combine to create unwanted results, as outlined in [Table 4](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#table4) below.  **7.4. Degradation with Device Age and Current:**Given the typical service life of industrial equipment, long-term reliability and consistent performance are becoming paramount concerns to system designers. Optocoupler timing parameters (e.g. propagation delay, pulse width distortion) can change with three different variables: 1) LED wear-out, 2) excessive LED input current; and 3) operating temperature.  One of the key optocoupler wear-out mechanisms is LED light output (LOP), a material-based phenomenon that causes the LED to lose brightness over time. Lower emission decreases the signal seen by the photo detector, negatively impacting optocoupler timing and output impedance characteristics. Figures 19A and 19B show manufacturer’s LOP data based on normalized light output over a period of 10,000 hours for LEDs made from both Gallium Arsenide Phosphide (GaAsP) and Aluminum Gallium Arsenide (AlGaAs), respectively. Light output degradation typically worsens with increasing temperature and increasing LED current. In the worst case, the light output can fall below the minimum value needed for proper device operation.   |  |  |  | | --- | --- | --- | | Optocoupler Manufacturer’s LOP Test Data for LEDs made from Gallium Arsenide Phosphide (GaAsP) |  | Optocoupler Manufacturer’s LOP Test Data for LEDs made from Aluminum Gallium Arsenide (AlGaAs) | | **Figure 19A. Optocoupler Manufacturer’s LOP Test Data for LEDs made from Gallium Arsenide Phosphide (GaAsP)** |  | **Figure 19B. Optocoupler Manufacturer’s LOP Test Data for LEDs made from Aluminum Gallium Arsenide (AlGaAs)** |   LOP can change nominal light output by as much as 20%, causing significant operating characteristic changes. Since the degradation rate is partially related to forward current, the system designer must take into account the effects of LOP when choosing the LED forward current operating range, forcing a trade-off between longer device service life and lower CMTI. The LOP wear-out precludes the use of optocouplers above approximately 100 °C and in 25 year lifetime applications, such as solar panels.  Section Summary: Many optocouplers have multiple, highly temperature-dependent parameters, such as the current transfer ratio and input turn-on and turn-off thresholds, which complicate design and negatively impact system performance. Optocouplers operating in electrically noisy environments commonly use additional external components to increase CMTI performance. Optocouplers also have both a narrower temperature operating range and inferior reliability (10x lower service life compared to CMOS digital isolators). By comparison, CMOS digital isolators are either on or off, eliminating the need for a CTR specification and its related temperature sensitivities; they have no wear-out mechanisms and possess tight input thresholds, superior CMTI, and greater parametric stability over temperature and current with industry-leading reliability.  [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top) | |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **8.0. Optocoupler Replacement Upgrades**  Optocouplers have traditionally dominated signal isolation applications because of the absence of alternative pin and package-compatible isolator solutions. The [Si87xx CMOS digital isolator](http://www.silabs.com/products/power/isolators/Pages/Si87xx-digital-isolators.aspx) (Figure 20) directly replaces optocouplers without PCB modification while providing significant gains in performance and reliability. The Si87xx input-side “harvests” input bias voltage from the Anode input while the output side is powered by a local voltage source of up to 30 Vdc. The Si87xx is also compatible with external optocoupler circuits, including those that implement the remedies shown in Figure 18.  Si87xx Optocoupler Replacement CMOS Digital Isolators  **Figure 20. Si87xx Optocoupler Replacement CMOS Digital Isolators**  The Si87xx input-side die includes a diode emulator, high-frequency transmitter and galvanic isolator stage. The diode emulator performs two functions: it mimics the behavior of an LED to ensure compatibility with existing (external) optocoupler input circuits, and it enables the transmitter when anode current is at or above its threshold value. When enabled, the transmitter propagates a high-frequency carrier across the isolation barrier to the receiver, which forces the output driver low when sufficient in-band energy is present. Conversely, input current below the threshold value disables the transmitter, causing the receiver to turn-off the open-drain MOSFET and allowing the external or internal pull-up resistor to pull the output pin high. This simple architecture provides a number of features and benefits over optocouplers:   * Package and pin-compatible, drop-in optocoupler upgrade with typically no PCB changes required * Silicon Labs patented CMOS isolation technology for higher performance and reliability * Isolation ratings: 3.75 kV and 5.0 kV * 10 kV surge tolerant per IEC 60065 * Faster, tighter timing: 1 Mbps or 15 Mbps versions, 60 ns prop delay, 20 ns PWD * CMTI: 35 kV/µs (A-Grade), or 50 kV/µs (B-Grade) and 2x to 3x lower internal parasitic coupling vs. optocouplers * Precise input current thresholds: 2.2 mA (A-Grade) and 3.5 mA (B-Grade) * No CTR * Very low parametric change with temperature * Wide -40 °C to +125 °C operating temperature range * High reliability: TDDB > 60 years at worst-case voltage and temperature   The Si87xx is based on the Industry-leading Si86xx and has substantially the same performance and reliability. Retrofitting an optocoupler consists of determining the appropriate Si87xx replacement, removing the existing optocoupler from its site, installing the Si87xx in its place, and verifying proper operation. Figure 21 shows such an upgrade where HCPL-4506 is replaced with an Si8712A.   |  |  |  | | --- | --- | --- | | Si87xx (Blue) vs. HCPL-4506 (Yellow) Performance Comparison at room temperature |  | Si87xx (Blue) vs. HCPL-4506 (Yellow) Performance comparison at 80°C | | **Figure 21A. Si87xx (Blue) vs. HCPL-4506 (Yellow) Performance Comparison at Room Temperature** |  | **Figure 21B. Si87xx (Blue) vs. HCPL-4506 (Yellow) Performance Comparison at 80°C** |   Test Board  **Si87xx and HCPL-4506 Test Board**  This test used an external digital signal connected to a BNC connector that is passed through a digital buffer and fed into the input pin of both the Si8712A digital isolator and the HCPL-4506-300E optocoupler. The output signals of both devices are connected to individual output test points allowing users to compare device performance on an oscilloscope. The oscilloscope photo of Figure 21A shows the two devices at room temperature, while Figure 21B shows device performance at 80 °C. Comparing these figures shows virtually no change to the performance of the Si8712A over temperature while the optocoupler both increases its propagation delay and loses much of its high-frequency content.  Table 4 summarizes common issues and solutions for digital optocouplers (Figure 18) and the Si86xx and Si87xx series of CMOS digital isolators. Note that the digital optocoupler relies on high current consumption to main CMTI, which decreases power efficiency and worsens wear-out due to LOP. The Si86xx logic input devices exhibit none of the issues found in digital optocouplers. The Si87xx devices have diode emulator input that mimics the behavior of an LED, including the potential need for higher input current, albeit a substantially lower current than optocouplers. | |
| |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **Table 4. Common Issues and Solutions for Optocouplers, and Si86xx and Si87xx CMOS Digital Isolators**   |  |  |  |  | | --- | --- | --- | --- | | **Issue** | **Digital Optocoupler Solutions** | **Si86xx CMOS Digital Isolators** | **Si87xx CMOS Digital Opto Retrofit Isolators** | | **Improve CMTI: Spurious Turn-On** | * Use optocoupler with higher thresholds * Add clamping diode or switch * Decrease value of RF(more current) * Increase value of CL(more current) * Decrease value of RL(more current) | * No issues | * Use higher threshold 87xx(B) versions * Decrease value of RF(more current) * Remove CL | | **Improve CMTI: Spurious Turn-Off** | * Decrease value of RF(more current) * Decrease value of RL(more current) | * No issues | * Use higher threshold 87xx(B) versions * Decrease value of RF(more current) * Increase value of RL | | **Decrease tPHL** | * Decrease value of RF(more current) * Increase value of RL * Decrease value of CL * Add peaking capacitor across RF | * No issues | * No issues | | **Decrease tPLH** | * Decrease value of RL(more current) * Decrease value of CL * Add peaking capacitor across RF | * No issues | * Decrease value of RL(more current) * Remove CL * No Issues | | **Address CTR Variation** | * Decrease value of RL(more current) | * No issues | * No issues | | **Address LED Aging Effects** | * Decrease value of RF(more current) | * No issues | * No issues |   **Notes:**   * All **"more current"** comments in **RED** refer to LED current only, and not output current. The **"more current"**comments in **BLUE** refer to output current. * If parasitic coupling through CLED01 and CLED02 causes Si87xxA false turn-on, replace Si87xxA with higher threshold Si87xxB. * Increasing CL requires more current for the same tPHL and tPLH. * Increasing RL requires more LED current for the optocoupler.   [Back to top](http://www.silabs.com/products/power/isolators/Pages/isolator-vs-optocoupler-technology.aspx#top) | |
| |  | | --- | | **Summary**  While optocouplers have been the dominant signal isolation solution for some time, the need for faster and more reliable, feature-rich isolation solutions is causing CMOS digital isolators to gain favor. [CMOS digital isolators](http://www.silabs.com/products/power/isolators/Pages/default.aspx)offer many significant benefits:   * Broad offering: Single, multi-channel (6 channels max), logic input and optocoupler replacement versions * Optocoupler upgrades: Advanced, drop-in optocoupler upgrades with higher performance and reliability * Tight timing performance: tPHL/tPLH, PWD, channel-to-channel skew, unit-to-unit matching and more… * High CMTI: up to 50 kV/µs * High reliability, longer service life: 60+ year TDDB * High surge immunity: 10 kV surge tolerant (Si87xx) * Stability: Very low parametric changes over operating temperature * Low EMI: meets FCC Class B Part 15 * Efficient: Low operating power per channel * High e-field immunity: Electric field immunity up to 50 V/m, magnetic field immunity above 1000 A/m Industry-leading ESD tolerance: up to 6 kV HBM * Ease of use: No CTR, 2x to 3x lower internal parasitics compared to optocouplers, intuitive device behavior   In conclusion, the benefits brought by CMOS [digital isolators](http://www.silabs.com/products/power/isolators/Pages/default.aspx) bring a high level of added value. The increases in performance, reliability and application ease make these devices unbeatable by products advanced by optocoupler manufacturers. | |