Digital Isolator Design Guide

This design guide helps system designers of galvanically isolated systems to begin designing with the Texas Instruments ISO72xx family of digital isolators in the shortest time possible. The document explains the basic operating principle of an isolator, suggests where to place it within a system design, and recommends guidelines for an electromagnetic compatible (EMC) circuit board design.

Further information is available in the ISO72xx data sheets and the ISO72xx EVM manuals.

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1 Operating Principle

The isolator in Figure 1 is based on a capacitive isolation barrier technique. The device consists of two data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to dc.

In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (*as in the case of a low-frequency signal*), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

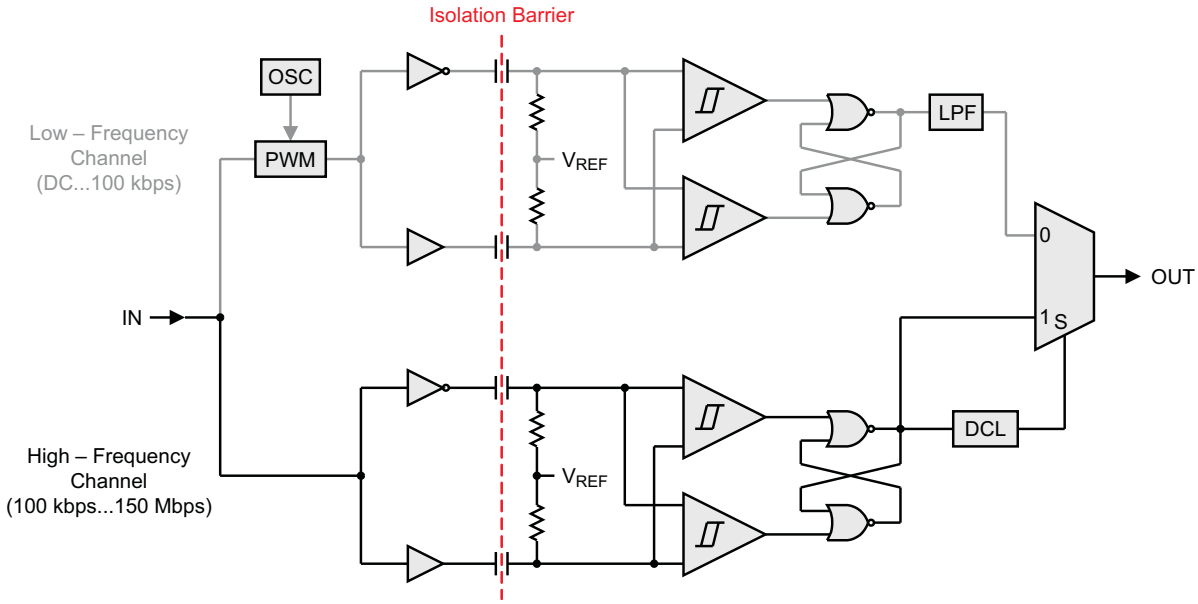


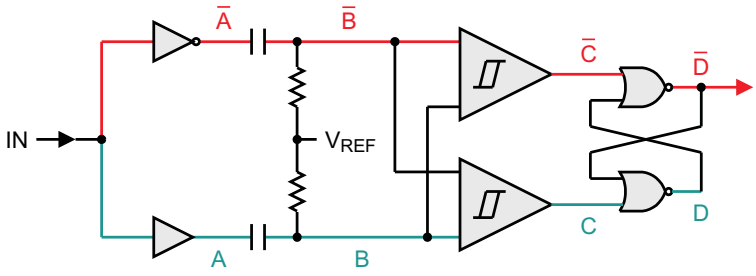
Figure 1. Internal Block Diagram of a Digital, Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

1.1 HF-Channel Operation

Figure 2 presents the high-frequency channel and the waveforms at specific points of the signal chain. The single-ended input signal is split into the differential signal components A and $\overline{A}$. Each signal component is then differentiated into the transients B and $\overline{B}$. The following comparators compare the differential transients to another. As long as the positive input of a comparator is on a higher potential than its negative input, the comparator output presents a logical High, thus converting an input transient into a short output pulse.

The output pulses set and reset a NOR-gate flip-flop. From the truth table, one sees that the NOR-gate configuration presents an inverting flip-flop, meaning that a High at input C sets output $\overline{D}$ to High, and a High at $\overline{C}$ sets D to High. Because the comparator output pulses are of short duration, sometimes both outputs are low. During this time, the flip-flop stores its previous output condition. Because the signal at $\overline{D}$ is identical in shape and phase with the input signal, $\overline{D}$ becomes the output of the high-speed channel and is connected to the output multiplexer.



C	$\overline{C}$	D	$\overline{D}$
L	L	S	S
L	H	H	L
H	L	L	H
H	H	L	L

S = store previous condition

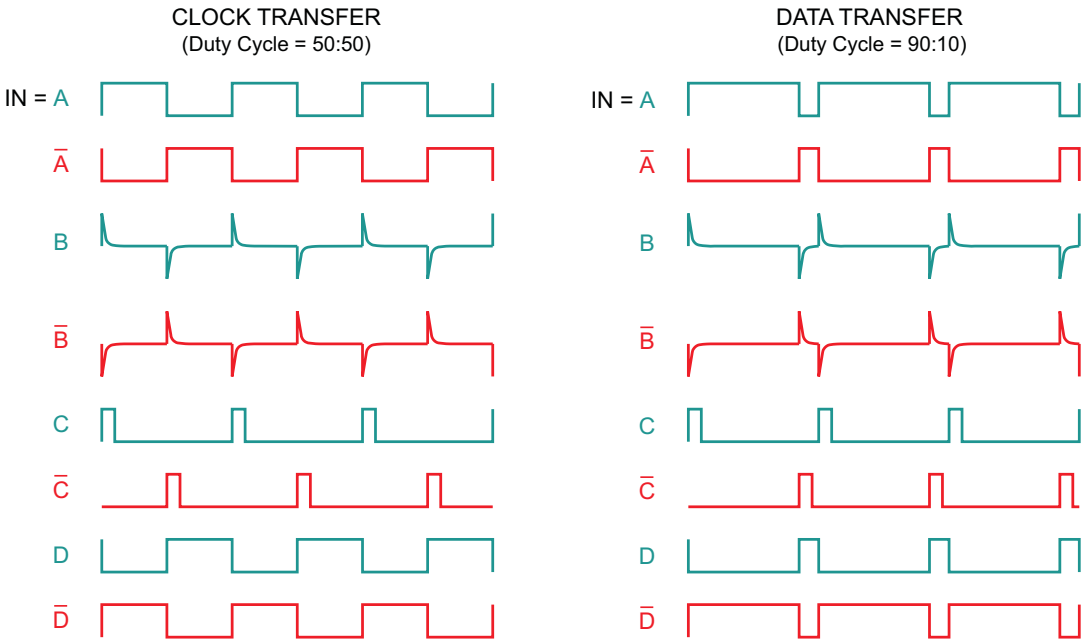


Figure 2. High-Frequency Channel Operation Timing

Whereas input signals with symmetric duty cycles cause equidistant pulses at the comparator outputs, unsymmetrical signals, (*shown in the right timing diagram of Figure 2*), move the comparator pulses closer to each other to maintain the shape and phase relationships of the input signal.

1.2 LF-Channel Operation

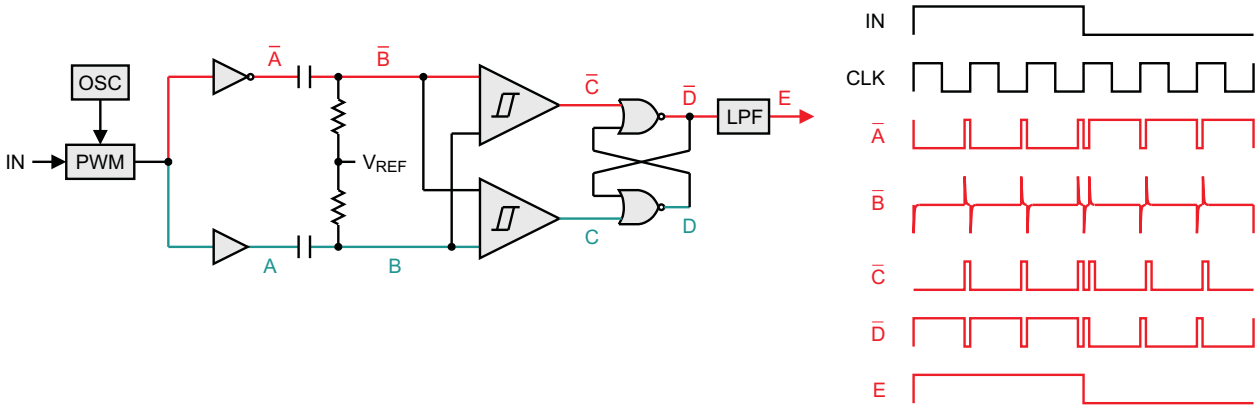


Figure 3. Low-Frequency Channel Operation Timing

Slow input signals are pulse-width modulated with a high-frequency carrier such, that a High-level yields a 90:10 duty cycle and a Low level a 10:90 duty cycle at location A. From there on, signal processing is identical with the asymmetrical signal processing in the high-speed channel. The only exception is, that the high-frequency content of the low-speed channel ($\overline{D}$) is filtered by an R-C low-pass filter before passed on to the output multiplexer (E).

2 Isolator Technology and Requirements

The successful proof of concept through the single isolator's capability of transmitting wideband data, (from dc to above 150 Mbps), inspired Texas Instruments to fabricate unidirectional and bidirectional devices in dual-, triple-, and quad-versions, that accommodate the most common digital interfaces encountered in industrial applications.

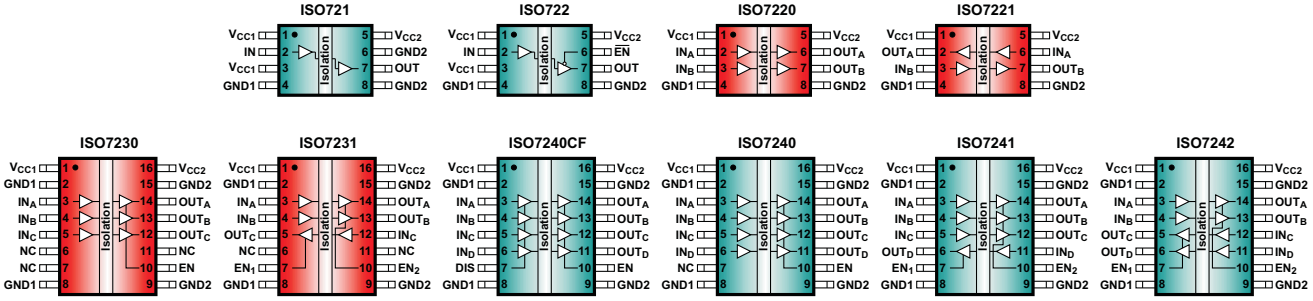


Figure 4. Overview of the Family of Stand-Alone Digital Isolators

All digital isolators use single-ended, 3-V/5-V CMOS-logic, switching technology. Their nominal supply voltage range is specified from 3.3 V to 5 V for both supplies, V_{CC1} and V_{CC2}, and allows any combination of these values.

When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended, 3-V/5-V digital signal lines.

Figure 5 to Figure 8 give examples of isolated interfaces for SPI, RS-232, and RS-485 applications. Note that the isolator is always placed between the data controller, (i.e., microcontroller or UART), and a data converter, or a line transceiver, regardless of the interface type or standard.

Figure 5 presents the most simple isolator application. Here the entire circuit constitutes a single-ended, low-voltage system in which a digital isolator connects the SPI interface of a controller with the SPI interface of a data converter. The most commonly applied isolators in SPI interfaces are ISO7231 and ISO7241, hence often designated as 3- and 4-channel SPI isolators.

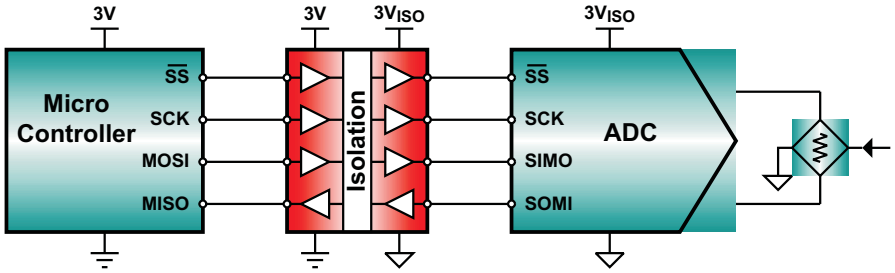


Figure 5. Isolated SPI Interface

The full-blown, isolated RS-232 interface in Figure 6 requires two quad isolators due to the six control signals required in addition to the actual data lines, RX and TX. Although the entire system is single-ended, the high-voltage requirements of the symmetric, ±13-V bus supply make it necessary to galvanically isolate the data link between the UART and the low-voltage side of the bus transceiver.

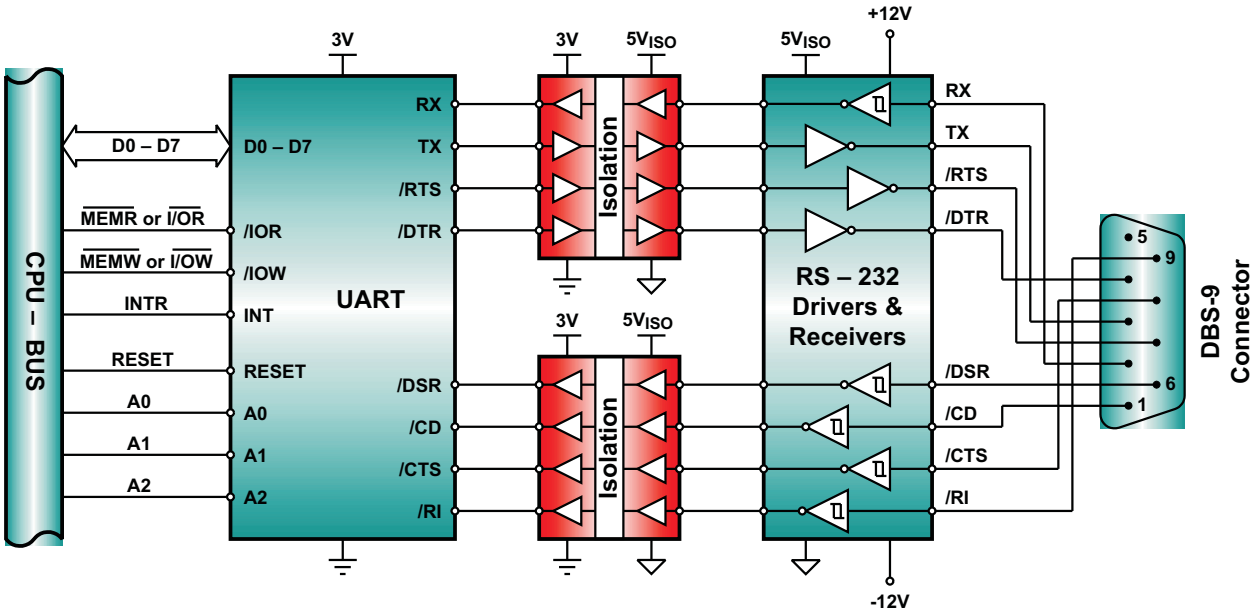


Figure 6. Isolated RS-232 Interface

As in the example in Figure 6, the isolation of the RS-485 interface in Figure 7 occurs between the controller and the bus transceiver. Despite the entire interface circuit being a low-volt system, the differential nature of the transmission bus requires prior isolation on the single-ended side.

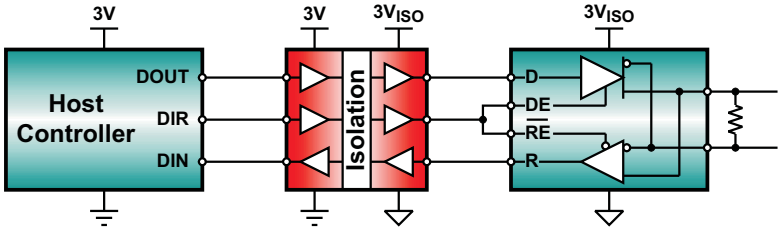


Figure 7. Isolated RS-485 Interface

Due to the simplicity of the interface shown in Figure 8, it was possible to integrate the isolator function into the transceiver circuit, thus providing an application-specific isolator device featuring low-cost and low component count.

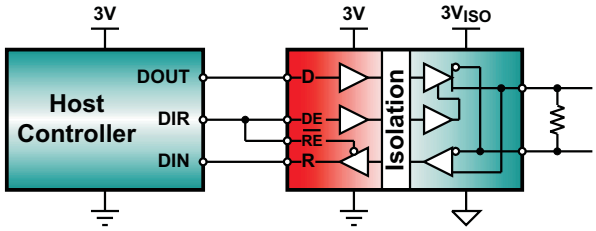


Figure 8. Integrated Isolated RS-485 Interface

To simplify the selection of an appropriate isolator for a specific application, Table 1 provides a comprehensive overview of Texas Instruments digital isolators.

Table 1. Overview of Stand-Alone and Application-Specific Isolators

Switching Characteristics for V_{CC1} = V_{CC2} = 5 V							
Isolator Type	**ISO**		**Input Threshold**	**Max. Data Rate [Mbps]**	**Max. Prop. Delay [ns]**	**Max. Ch / Ch Output Skew [ns]**	**Typ. Output Rise Time [ns]**
Single	721 / 722		TTL	100	24	–	1
		M	CMOS	150	16	–	1
Dual	7220, 7221	A	TTL	1	475	15	1
		B		5	70	3	1
		C		25	42	1	1
		M	CMOS	150	16	1	1
Triple	7230, 7231	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
Quad	7240, 7241, 7242	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
	7240	CF	TTL	25	42	2	2
RS-485 Half Duplex	3082		TTL	0.2	1.3 (XTR) 125 (RCV)	–	900 (XTR) 1 (RCV)
	15		TTL	1	340 (XTR) 100 (RCV)	–	185 (XTR2) 2 (RCV)
	3088		TTL	20	45 (XTR) 125 (RCV)	–	7 (XTR1) 1 (RCV)
RS-485 Full Duplex	3080		TTL	0.2	1.3 (XTR) 125 (RCV)	–	900 (XTR1) 1 (RCV)
	35		TTL	1	340 (XTR) 100 (RCV)	–	185 (XTR2) 2 (RCV)
	3086		TTL	20	45 (XTR) 125 (RCV)	–	7 (XTR1) 1 (RCV)
Profibus Half-Duplex	1176		–	40	40 (XTR) 55 (RCV)	1	3 (XTR) 2 (RCV)

Of the five different speed grades for isolators, A, B, C, CF, and M, only the A, B, C, and CF versions possess internal low-pass noise filters at the data inputs and are therefore recommended for use in noisy environments. The high-speed version, M, requires external input filtering when used in noisy environments. This is accomplished by connecting a filter capacitor from an input to the respective device ground. The capacitor value is calculated via $C_F = 1/ (2\pi f_{max} \times R_S)$, with f_{max} as the maximum signal frequency and R_S as the output impedance of the signal source.

3 PCB Design Guidelines

3.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as printed-circuit board (PCB) material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0 and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing, flammability characteristics.

3.2 Layer Stack

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 9). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.

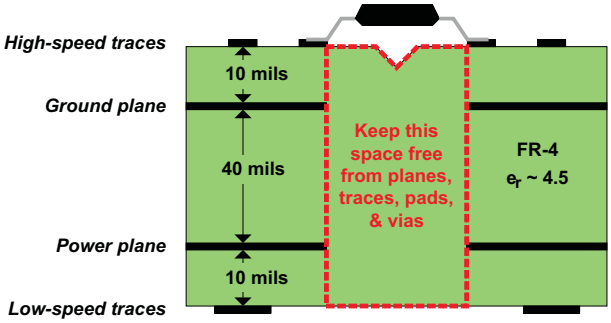


Figure 9. Recommended Layer Stack

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

3.3 Creepage Distance

Creepage distance is the shortest path between two conductive parts measured along the surface of the insulation. An adequate creepage distance protects against tracking, a process that produces a partially conducting path of localized deterioration on the surface of an insulating material as a result of the electric discharges on or close to an insulation surface.

The degree of tracking occurring depends on the comparative tracking index (CTI) of the material and the degree of pollution in the environment. Used for electrical insulating materials, the CTI provides a numerical value of the voltage that will cause failure by tracking during standard testing. IEC 112 provides a fuller explanation of tracking and CTI.

Tracking damaging the insulating material normally occurs because of one or more of the following reasons: humidity in the atmosphere, presence of contamination, corrosive chemicals, and altitude at which equipment is to be operated.

As isolation voltage levels continue to rise, it is more important than ever to have a robust PCB design that not only reduces electromagnetic interference emissions, but also reduces creepage problems. In addition to wide isolator packaging, techniques such as grooves can be used to attain a desired creepage distance (see Figure 10).

Figure 10. Groove Cutting Extends Effective Creepage Distance

For a groove (>1 mm wide), the only depth requirement is that the existing creepage distance plus the width of the groove and twice the depth of the groove must equal or exceed the required creepage distance. The groove must not weaken the substrate to a point that it fails to meet mechanical test requirements.

Also, on all layers keep the space under the isolator free from traces, vias, and pads to maintain maximum creepage distance (see Figure 9).

3.4 Controlled Impedance Transmission Lines

A controlled impedance transmission line is a trace whose characteristic impedance, Z_0, is tightly controlled by the trace geometries. In general, these traces match the differential impedance of the transmission medium, such as cables and line terminators, to minimize signal reflections. Around digital isolators, controlled impedance traces must match the isolator output impedance, $Z_0 \sim r_O$, which is known as source-impedance matching.

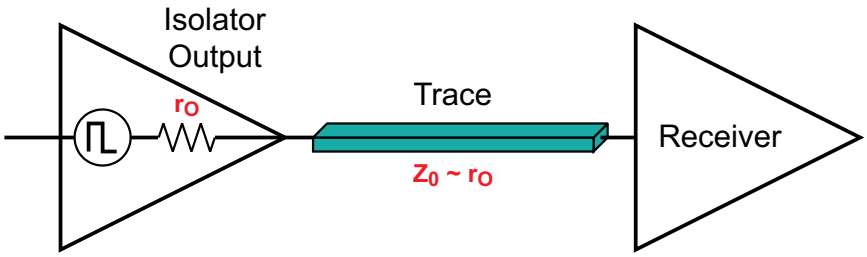


Figure 11. Source Impedance Matching: $Z_0 \sim r_O$

To determine Z_0, the dynamic output impedance of the isolator, $r_O = \Delta V_{OUT}/\Delta I_{OUT}$, needs to be established. For that purpose the output characteristic in Figure 12, (*taken from the ISO7240 data sheet*), is approximated by two linear segments indicating an $r_O \sim 260\ \Omega$ at low voltages, while for the majority of the curve, (*and thus the transition region of the output*), $r_O \sim 70\ \Omega$.

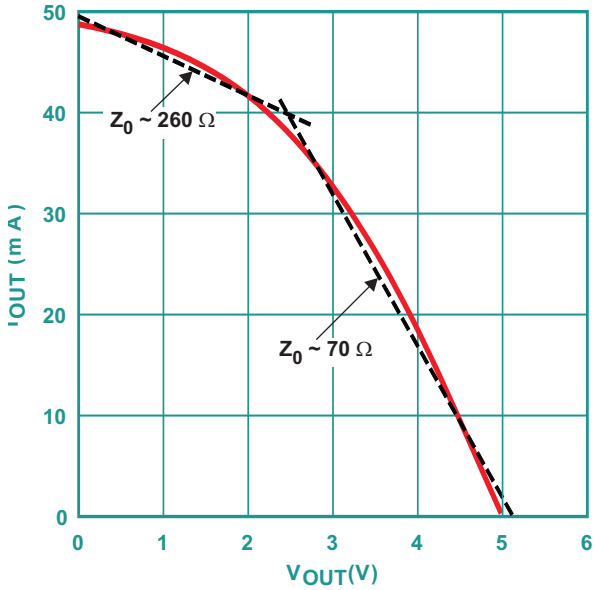


Figure 12. Isolator Output Characteristic

The required trace geometries, such as trace thickness (t) and width (w), the distance between trace and an adjacent ground layer (d), and the PCB dielectric (ε_r), are partially dictated by the copper-plating capabilities of the board manufacturing process and the dielectric of the chosen board material. Typical values are 1 and 2 oz of copper-plating, resulting in trace thicknesses of t = 1.37 mils and t = 2.74 mils, respectively. Dielectric values for FR-4 epoxy-glass vary between ε_r = 2.8 to 4.5 for microstrip, and ε_r = 4.5 for stripline traces.

With t and ε_r given, the designer has the freedom to define Z_0 through trace width w, and distance d. For PCB designs, however, the most critical dimensions are not the absolute values of w and d, but their ratio w/d. Easing the designer's task, Figure 13 plots the characteristic trace impedance as a function of the width-to-height (w/h) for a trace thickness of 2.74 mils (2-oz copper plating), an FR-4 dielectric of 4.5, and a trace-height of 10 mils above the ground plane.

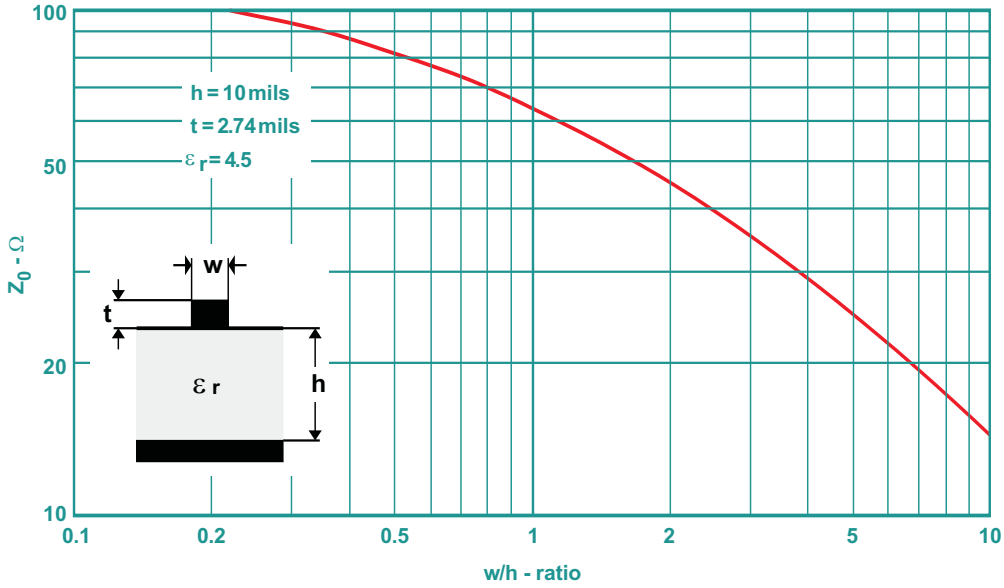


Figure 13. Characteristic Impedance as a Function of the w/h Ratio

From Figure 13 it is apparent that a 70-Ω design requires a w/h ratio of about 0.8. As described in the

following section, *Reference Planes*, designing a low EMI board requires close electric coupling between signal trace and ground plane, which is accomplished by ensuring that h = 10 mils. The corresponding trace-width is therefore 8 mils. This width must be maintained across the entire trace length. Otherwise, variations in trace width cause discontinuities in the characteristic impedance, thus leading to increased reflections and EMI.

Note, that the preceding design example is only one of many possibilities to achieve the desired Z_0. Different trace thickness due to higher or lower copper plating, or different PCB material can be used, but require the w/d ratio to change. The rather complex, mathematic equations for calculating the characteristic impedance Z_0, while taking trace thickness, width, and dielectric into account, are presented in Table 2.

Table 2. Microstrip Equations for 0.2 < w/d < 1

$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \times \left[\frac{1}{\sqrt{1 + \frac{12 \times h}{w}}} + 0.04 \times \left(1 - \frac{w}{h}\right)^2 - \frac{t}{2.3 \times \sqrt{w \times h}} \right]$	ε_{eff} = effective dielectric, taking into account: • dielectric of air • dielectric of PCB material • height above ground • nominal trace width
$w_{eff} = w + \frac{1.25 \times t}{\pi} \times \left[1 + \ln\left(\frac{2 \times h}{t}\right)\right]$	w_{eff} = effective trace width, taking into account: • nominal trace width • trace thickness • height above ground
$Z_0 = \frac{60 \times \ln\left(\frac{8 \times h}{w_{eff}} + \frac{w_{eff}}{4 \times h}\right)}{\sqrt{\varepsilon_{eff}}}$	Z_0 = characteristic impedance, taking into account: • effective trace width • height above ground • effective dielectric
Note: Keep all dimensions in inch, or mils (1 in = 1000 mils), or mm (1 in = 25.4 mm).	

3.5 Reference Planes

The power and ground planes of a high-speed PCB design usually must satisfy a variety of requirements.

At dc and low frequencies, they must deliver stable reference voltages, such as V_{CC} and ground, to the supply terminals of integrated circuits (IC).

At high frequencies reference planes, and in particular ground planes, serve numerous purposes. For the design of controlled impedance transmission systems, the ground plane must provide strong electric coupling with the signal traces of an adjacent signal layer.

Consider a single, ac-carrying conductor with its associated electric and magnetic fields, shown in Figure 14. Loose or no electric coupling allows the transversal electromagnetic (TEM) wave, created by the current flow, to freely radiate into the outside environment, causing severe electromagnetic interference (EMI).

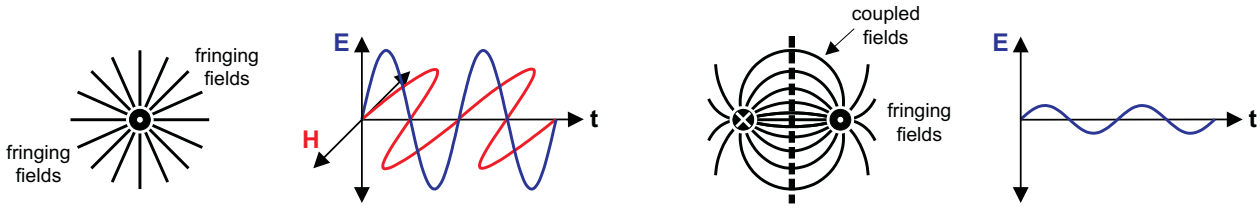


Figure 14. Reducing Field Fringing Through Close Electric Coupling Between Conductors

Now imagine a second conductor in close proximity, carrying a current of equal amplitude but opposite polarity. In this case, the conductors' opposing magnetic fields cancel, while their electric fields tightly couple. The TEM waves of the two conductors, now being robbed of their magnetic fields, cannot radiate into the environment. Only the far smaller fringing fields might be able to couple outside, thus yielding significantly lower EMI.

Figure 15 shows the same effect occurring between a ground plane and a closely coupled signal trace. High-frequency currents follow the path of least inductance, not the path of least impedance. Because the return path of least inductance lies directly under a signal trace, returning signal currents tend to follow this path. The confined flow of return current creates a region of high current density in the ground plane, right below the signal trace. This ground plane region then acts as a single return trace, allowing the magnetic fields to cancel while providing tight electric coupling to the signal trace above.

Figure 15. Ground Plane Acting as a Single Return Trace

To provide a continuous, low-impedance path for return currents, reference planes (power and ground planes) must be of solid copper sheets and free from voids and crevices. For reference planes, it is important that the clearance sections of vias do not interfere with the path of the return current. In the case of an obstacle, the return current finds its way around it. However, by doing so, the current's electromagnetic fields will most likely interfere with the fields of other signal traces introducing crosstalk. Moreover, this obstacle adversely affects the impedance of the traces passing over it, thus leading to discontinuities and increased EMI.

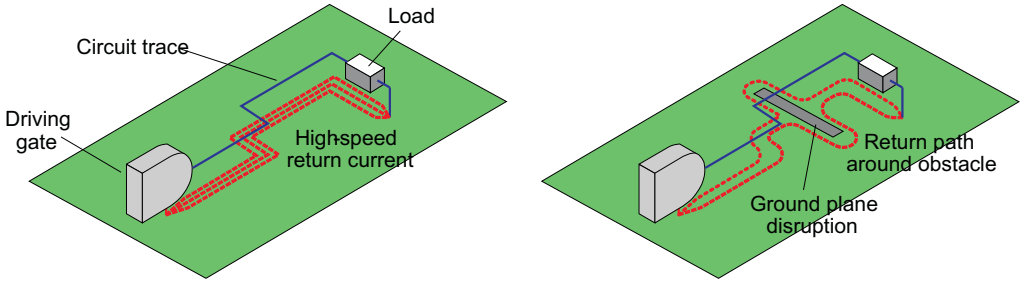


Figure 16. Return Current Paths in Solid Versus Slotted Ground Planes

3.6 Routing

Guidelines for routing PCB traces and placing components are necessary when trying to maintain signal integrity, avoiding noise pick-up, and lower EMI. Although an endless number of precautions seems to be taken, this section provides only a few main recommendations as layout guidance.

1. Keep signal traces 3 times the trace-to-ground height, (d = 3h), apart to reduce crosstalk down to 10%. Because the return current density under a signal trace diminishes via a $1/ [1+(d/h)^2]$ function, its density at a point d > 3h, is sufficiently small to avoid causing significant crosstalk in an adjacent trace.

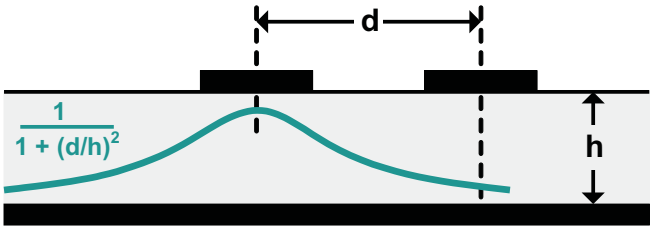


Figure 17. Separate Traces to Minimize Crosstalk

2. Use 45° bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, and thus the trace impedance. This creates additional impedance mismatch, which may lead to higher reflections.

Figure 18. Use 45° Bends Instead of 90° Bends

3. For permanent operation in noisy environments, connect the Enable inputs of an isolator through a via to the appropriate reference plane, that is, High-Enable inputs to the V_{CC} plane and Low-Enable inputs to the ground plane.
4. When routing traces next to a via or between an array of vias, ensure that the via clearance section does not interrupt the path of the return current on the ground plane below. If a via clearance section lies in the return path, the return current finds a path of least inductance around it. By doing so, it may cross below other signal traces, thus generating cross-talk and increase EMI.

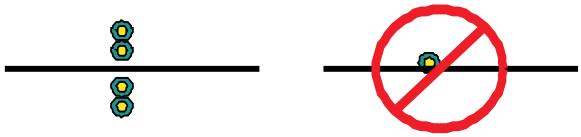


Figure 19. Avoiding via Clearance Sections

5. Avoid changing layers with signal traces as this causes the inductance of the signal path to increase.
6. If, however, signal trace routing over different layers is unavoidable, accompany each signal trace via with a return-trace via. In this case, use the smallest via size possible to keep the increase in inductance at a minimum.
7. Use solid power and ground planes for impedance control and minimum power noise.
8. Use short trace lengths between isolator and surrounding circuits to avoid noise pick-up. Digital isolators are usually accompanied by isolated dc-to-dc converters, providing supply power across the isolation barrier. Because single-ended transmission signaling is sensitive to noise pick-up, the switching frequencies of close-by dc-to-dc converters can be easily picked up by long signal traces.
9. Place bulk capacitors, (i.e., 10 µF), close to power sources, such as voltage regulators or where the power is supplied to the PCB.
10. Place smaller 0.1-µF or 0.01-µF bypass capacitors at the device by connecting the power-side of the capacitor directly to the supply terminal of the device and through two vias to the V_{cc} plane, and the ground-side of the capacitor through two vias to the ground plane.

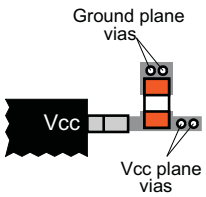


Figure 20. Connect Bypass Capacitor Directly to V_{cc} Terminal

3.7 Vias

The term via commonly refers to a plated hole in a printed-circuit board. Although some applications require through-hole vias to be wide enough to accommodate the leads of through-hole components, high-speed board designs mainly use them as trace routing vias when changing signal layers, or as connecting vias to connect SMT components to the required reference plane, and also to connect reference planes of the same potential to each other.

Layers connecting to a via do so by making direct contact with a pad surrounding the via, (the via pad). Layers that must not connect are separated by a clearance ring. Every via has a capacitance to ground which can be approximated using the following equation:

$$C = \frac{1.41 \times \varepsilon_r \times T \times D_1}{D_2 - D_1} \quad (1)$$

Where

D_2 = diameter of clearance hole in ground planes, [in.].
D_1 = diameter of pad surround via, [in.].
T = thickness of printed circuit board, [in.].
ε_r = dielectric constant of the circuit board.
C = parasitic via capacitance, [pF].

Because the capacitance increases proportional with size, trace vias in high-speed designs must be as small as possible to avoid signal degradation caused by heavy capacitive loading.

When connecting decoupling capacitors to a ground plane or interconnecting ground planes, the via inductance becomes more important than its capacitance. The magnitude of this inductance is approximately:

$$L = 5.08 \times h \times \left[\ln\left(\frac{4 \times h}{d} \right) + 1 \right] \quad (2)$$

Where

L = via inductance, [nH].
h = via length, [in.].
d = via diameter, [in.].

Because this equation involves a logarithm, changing the via diameter does little to influence the inductance. A big change may be effected by changing the via length or by using multiple vias in parallel. Therefore, connect decoupling capacitors to ground by using two paralleled vias per device terminal. For low inductance connections between ground planes, use multiple vias in regular intervals across the board.

Although it is highly recommended not to change layers of high-speed traces, if the necessity still occurs, ensure a continuous return current path. Figure 21 on the left shows the flow of the return current for a single layer change and on the right for a multiple layer change.

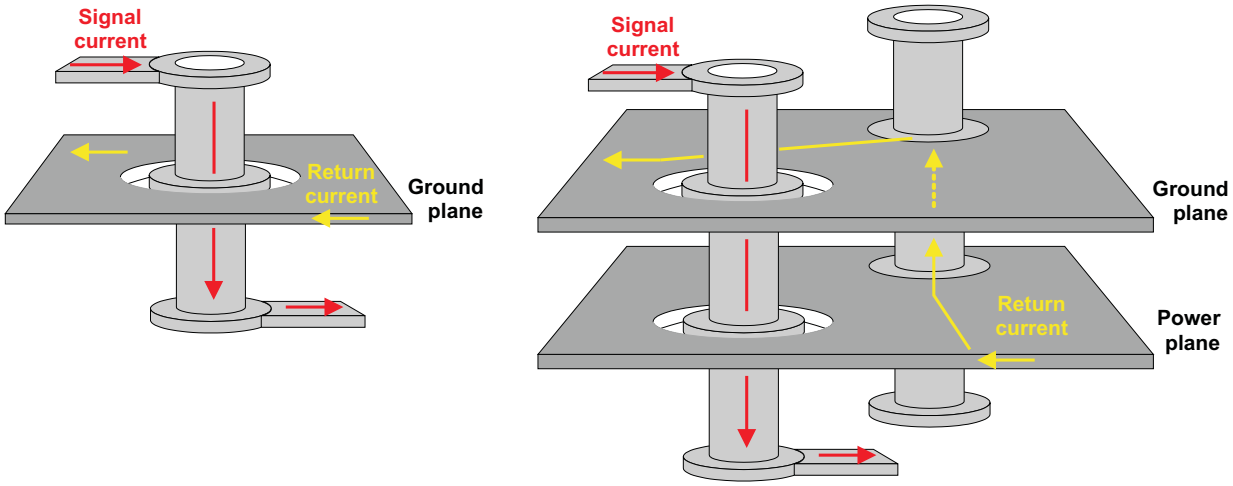


Figure 21. Return Current Paths for a Single and a Multiple Layer Change

The ability for the current flow to change from the bottom to the top of the ground plane is provided by a metallic laminate of the inner clearance ring. Thus, when a signal passes through a via and continues on the opposite side of the same plane, a return current discontinuity does not exist.

Changing a signal trace from one layer to another by crossing multiple reference planes complicates the design of the return current path. In the case of two ground planes, a ground-to-ground via must be placed near the signal via to ensure a continuous return current path, (right diagram in Figure 21).

If the reference planes are of different voltage potentials, such as the power and ground planes in Figure 22, the design of the return path becomes messy as it requires a third via and a decoupling capacitor. The return current flow begins at the bottom of the power plane, where it is closest to the signal current. It then flows through the power via, across the decoupling capacitor into the ground via and returns on top of the ground plane.

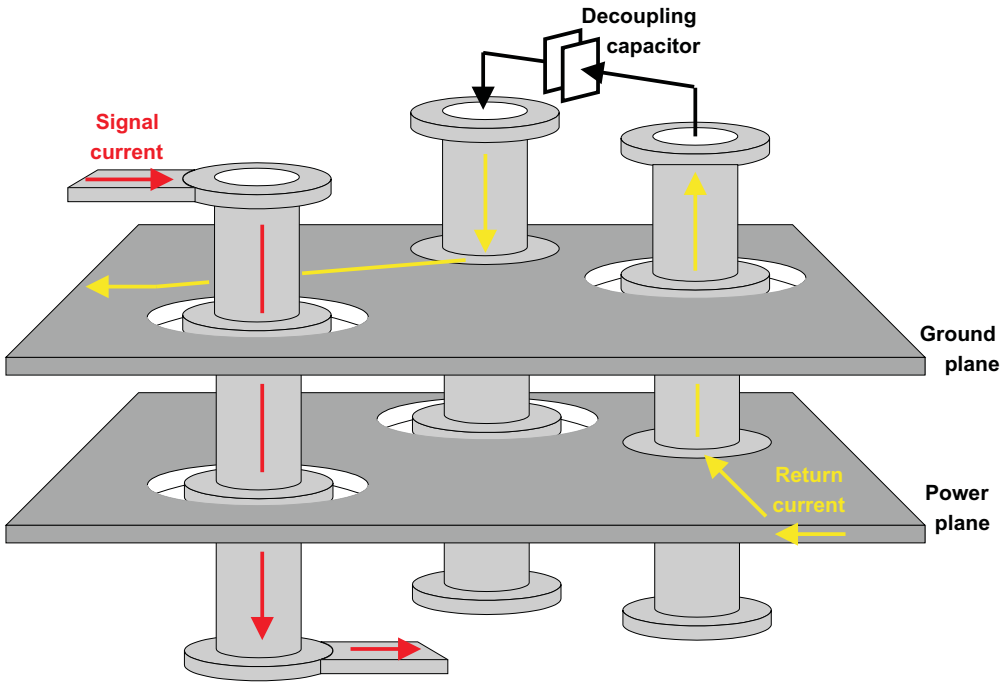


Figure 22. Return Current Paths for a Single and a Multiple Layer Change

Current return paths comprising multiple vias and decoupling capacitors possess high inductance, thus compromising signal integrity and increasing EMI. If possible, avoid changing layers during high-speed trace routing, as it usually worsens board performance, complicates design, and increases manufacturing cost.

3.8 Decoupling Capacitors

Decoupling capacitors provide a local source of charge for ICs requiring a significant amount of supply current in response to internal switching. Insufficient decoupling causes a lack of supply current required which may prevent the IC from working properly, resulting in signal integrity data errors to occur. This requires them to provide low impedance across the frequency range of interest. To accomplish that, a common approach is to distribute an array of decoupling capacitors evenly across the board. In addition to maintaining signal integrity, decoupling capacitors serve as EMC filters preventing high-frequency RF signals from propagating throughout the PCB.

When connecting a capacitor between the power and ground planes, the power supply is actually loaded with a series resonant circuit, whose frequency dependent R-L-C components represent the equivalent circuit of a real capacitor. Figure 23 shows the parasitic components of an initial equivalent circuit and their conversion into a series resonant circuit.

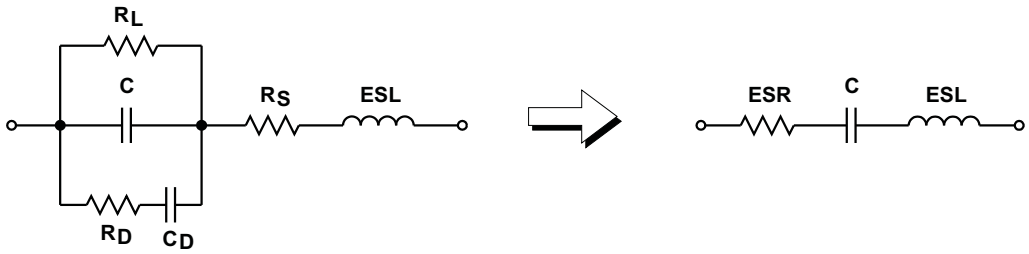


Figure 23. Capacitor Losses Modeled by a Series Resonance Circuit

The leakage resistance R_L represents the loss through leakage current at low frequencies. R_D and C_D indicate the losses due to molecular polarization, (R_D), and dielectric absorption, (C_D). R_S depicts the resistance in the leads and the plates of the capacitor. The three resistive losses are combined into one equivalent series resistance (ESR). As in the ESR case, the equivalent series inductance (ESL) combines the inductance of the capacitor plates and the internal leads.

Note that the capacitor connecting vias, although low in impedance, contribute a significant amount to the series inductance. Therefore, reduce via inductance by using two vias per capacitor terminal.

Figure 24 shows the progression of capacitor impedance (Z) versus frequency for a 10-nF capacitor. At frequencies far below the self-resonance frequency (SRF), the capacitive reactance is dominant. Closer to SRF, the inductive reactance gains influence trying to neutralize the capacitive component. At SRF, the capacitive and inductive reactance cancel, and only the ESR is effective. Note that the ESR is frequency dependent, and contrary to popular belief, does not reach its minimum at SRF. The impedance Z, however, does.

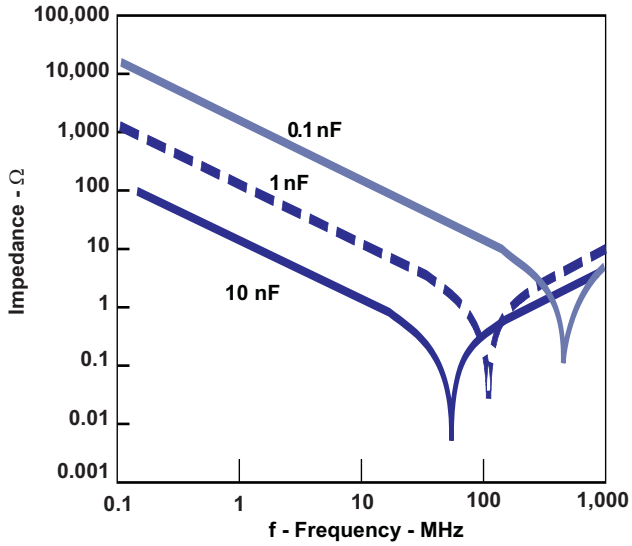


Figure 24. Capacitor Impedance Versus Frequency

The reason why the paralleling of capacitors in a distributed decoupling network works is because the total capacitance increases to $C_{TOT} = C \times n$, where n is the number of decoupling capacitors used. And with $X_c = 1/(\omega \times C)$, the capacitor impedance is reduced to $X_c = 1/(n \times \omega \times C)$ for frequencies below SRF. Similarly, this holds true for the inductance. Here $L_{TOT} = L/n$, and because $X_L = \omega \times L$, the impedance decreases to $X_L = \omega \times L/n$ for frequencies above SRF.

Designing a solid decoupling network must include lower frequencies down to dc, which requires the implementation of large bypass capacitors. Therefore, to provide sufficient low impedance at low frequencies, place 1-µF to 10-µF tantalum capacitors at the output of voltage regulators and at the point where power is supplied to the PCB. For the higher frequency range, place several 0.1-µF or 0.01-µF ceramic capacitors next to every high-speed switching IC.

4 Summary

The objective of this design guide is to cover the main aspects of PCB design with digital isolators. Despite the enormous amount of technical literature, seminars, newsletters and internet forums on PCB design, this document provides designers with layout guidelines in a comprehensive way. By following the recommendations presented herein, designers can accomplish EMC-compliant board design in the shortest time possible.

5 References

1. High-speed Digital Design, Johnson/Graham, 1993
2. Noise Reduction Techniques in Electronic Systems, Ott, 1988
3. Eliminating the myths about printed circuit board power/ground plane decoupling, Archambeault, 2001.

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