An innovative low-cost device for electricity metering services

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Abstract: The paper presents a prototype of cost-effective device mandated to identify, classify and measuring typical disturbances characterizing the quality of power supply systems. In particular, variations from the nominal root-mean-square value of the voltage signal, referred to as sag, interruption and swell, are taken into account. Moreover, specific functionalities implemented on the prototype offer the possibility of measuring the apparent and active absorbed by a connected load, as well as verifying voltage spectral purity by mean of the evaluation of a traditional total harmonic distortion index.

I. INTRODUCTION

Thanks to the recent modernization of the electric network, mainly stimulated by the possibilities offered by power electronics, new capabilities in the distribution of electricity have been accomplished and exploited by providers, as well as new optimized modes of energy utilization have been pursued and set up by customers. Unfortunately, although modernization has assured several benefits, involving energy savings and improved safety, the number of faults and malfunctioning revealed by factory and domestic customers has increased, because of major sensitivity to power quality disturbances exhibited by the new-deployed electronic equipment [1]-[7].

Electricity providers and customers are, indeed, paying more and more attention to the quality features of electricity. Among them, medium and small factory customers, which have neither skill nor proficiency in presiding over their electric network, usually contract business with qualified electricians to achieve regular maintenance and punctual intervention in the case of any trouble with energy provision and utilization. Committed electricians are thus given the task of looking into strategies and for devices to evaluate electric energy efficiency and detect power quality deterioration; their main goal is to prevent any interruption of the industrial process due to electric malfunctioning.

To achieve the aforementioned goal, the deployment of state-of-art systems for continuous monitoring and data logging of electricity parameters would be precious [8]. These systems, referred to as power quality analyzers, combine the functionalities present in digital oscilloscope characterized by massive data recording capabilities with those offered by digital multimeters. They permit the detection and classification of momentary interruptions, sags, and swells. They also provide estimates of frequency bias and fluctuations, flicker, harmonic, and interharmonic distortion. The most expensive ones offer multiple inputs for contemporaneous analyses up to six phases, and allow synchronisation between ensembles of analyzers through the GPS system in order to solve tasks involving distributed monitoring operations. Some of them are even complemented with signalling capabilities for data transmission to remote databases where reports concerning electric energy demand and consumption, hourly, daily, and weekly profiles of electric quantities, number of supply interruptions occurred during a limited period, and records of timing and duration of any anomaly that could preclude to equipment failures or other sort of malfunctioning can be hosted and analyzed. Anyway, the cost of a state-of-art monitoring system for electric networks is still prohibitive for medium and small customers.

The available data are, however, just those provided onsite by the particular permanently installed instrument for measurement of electricity. Unfortunately, the most popular instrument installed on site is the low-cost utility revenue or billing meter, which lacks of the major functionalities offered by power quality analyzers; in particular, it has no data storage capabilities or very poor ones, which allow the collection of a few parameters related to energy consumption and demand, but neither hourly or daily or weekly profiles of the electrical parameters. So, electricians engaged in maintenance and troubleshooting tasks must utilize portable power quality analyzers for the execution of tests on electric apparatuses connected to the distribution network. Thus they can only refer to data acquired during either regular visits, which are scheduled according to a specific maintenance program, or occasional inspections, which are required successively to faulty events.

At present, electricians claim for low-cost devices [9], retailed for their clients, with a restricted number of functionalities and minor configurable options with respect to that offered by power quality analyzers to suit the peculiarity of their customers. It is worth noting that, although guidelines to the design of electronic meters have recently been published by major electronics vendors [10], all the

investments needed to develop, construct, and customize electricity meters to meet specific requirements is still far beyond the capabilities of the involved operators.
The paper presents a low-cost device for electricity metering service that satisfies the needs of electricians engaged in maintenance programs contracted with small and medium factories. The proposed device is low cost and can be easily integrated in the electric distribution network. It consists of a set of units, each of which made up of suitable transducers for preconditioning current and voltage waveforms observed in the electric network, a multiplexed analog-to-digital converter for digitizing the aforementioned waveforms, and a processing unit complemented with memory registers for indexes and parameters estimation. Each unit is also equipped with a mass-storage memory, such as a memory card, in order to allow regular downloading of detailed data reports. Data download can be approached during the regular inspections necessary to control electric apparatuses usage and consumption.

II. HARDWARE ARCHITECTURE

A low-cost device for electricity measurement service has been realized (Fig. 1). The main element is the digital signal controller DSC, *dsPIC30F6010* by Microchip (120 MHz maximum clock frequency, 30 MIPs, million of instructions per second, 144 KB on-chip Flash program space, 8 KB of on-chip data RAM, 4 KB of non-volatile data EEPROM, 10-bit analog-to-digital converter, 5 independent Timers, each of which can be used as interrupt source). The dsPICDEM™ board, namely the system provided by Microchip for evaluating dsPIC® microcontroller, has been used to access the I/O pins of DSC. Thanks to a suitable front-end realized through proper electronic transducers (Fig. 2) and suitable measurement algorithms, described in detail in Section III, the device is capable of assuring reliable detection of typical power quality events (i.e. sag, swell, and interruption) as well as performing accurate measurement of voltage total harmonic distortion (THD) and power, both active and apparent, absorbed by the load.

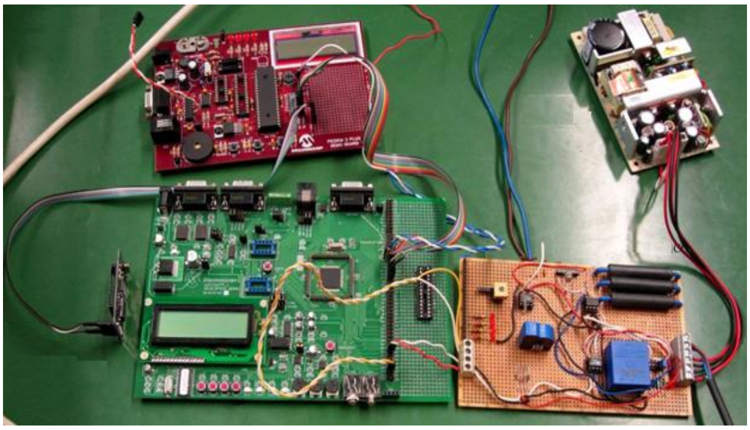

Figure 1 – Current version of the realized device prototype.

The realized front-end is made up of two sections (Fig. 2) mandated to condition the waveforms of line voltage and current, respectively. Two Hall effect transducers have been preferred for both measurement of current and voltage amplitude. With respect to other commercial solution available on the market, these transducers present, in fact, the following advantages: (i) high accuracy over wide ranges both of amplitude and frequency, (ii) galvanic insulation between the power network and measuring circuits, (iii) low cost-performance ratio.
The adopted voltage transducer is a *LV 25-P* by LEM [11] (0.9% accuracy, 0.2% linearity error, DC-100kHz bandwidth). According to the transducer specifications, a suitable resistor R_1 is connected to the input in order to fix the nominal root-mean-square (RMS) value of input current to 10 mA (corresponding to an RMS voltage of 230 V). The transducer output is a current, the RMS value of which is within a range 0-25 mA directly related to the input line-neutral voltage. The output signal is, then, gathered as voltage drop across a high precision resistance R_M (Fig. 2), the value of which is equal to 51 Ω. Since the analog-to-digital converter of the adopted DSC is unipolar, a positive voltage, equal to 2.5 V and provided by a voltage reference, is added to adequately adapt the mean value of ADC input voltage.
The current transducer is a *LTS 6-NP* by LEM [12] (0.2% accuracy, 0.1% linearity error, DC-100kHz bandwidth). The transducer output is a voltage related to the primary current I_P according to the following expression, $V_{out} = 2.5 \pm 0.625 \frac{I_P}{I_{PN}}$, where I_{PN}=15 A is the nominal primary current. For this transducer, then, the provided voltage signal can be straightforwardly digitized by the ADC of the adopted DSC and no further signal conditioning is required.
According to the whole layout of the device shown in Fig. 3, a further microcontroller, namely *PIC18F452* (in the following referred to as PIC) by Microchip, is, finally, linked to the DSC through a parallel connection and acts as communication interface for data storage. Measurement results are, in fact, collected and saved in an external storage unit, i.e. memory card, for data logging purpose.

III. SOFTWARE ARCHITECTURE

The dsPICDEM™ evaluation system has been used in conjunction with MPLAB 7.40™ development environment in order to (i) implement in mixed code both measurement algorithms and control software, (ii) program, and (iii) debug DSC. As stated above, the measurement scheme aims at (i) detecting the occurrence of typical power quality events, (ii) measuring their duration, (iii) controlling useful parameters such as voltage total harmonic distortion and active and apparent power absorbed by a load. The operating scheme of the DSC is based on a finite states machine (FSM), the details of which are given in the following, along with some indications of the other implemented functions. In order to assure the best performance in terms of computational burden and speed of execution, all the code needed to device functioning has been written in assembly, but the portion, included in the main function, accounting for the FSM. Moreover, fixed point arithmetic has been used due to its inherent implementation on DSC; floating point operations have, in fact, to be software executed, thus involving a further computational burden.

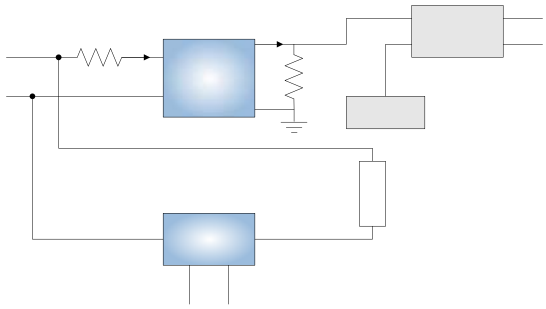

Figure 2 – Electrical scheme of developed analog front-end.

Operating functionalities of the DSC can be divided in two main categories: initialization and measurement functions.

A. Initialization

The first stage of the software architecture is mandated to the initialization and management of DSC. As specified below, three different timers (Timer 3, Timer 4, and Timer 5) are used to correctly execute the whole measurement procedure. In particular, they are, respectively, exploited to control (*i*) sampling period, (*ii*) blanking time (i.e. the initial time interval during which the device operations are turned off), and (*iii*) time interval between successive THD or power measurements. The memory portion mandated to collect acquired samples is also fixed and initialized in this stage. In particular, voltage samples are collected in a 256-points record, while current samples are stored in 128-points memory buffer. Thanks to the facilities provided by the adopted DSC, the management of both buffers is transparently accomplished by the DSC itself according to a standard first-in-first-out strategy.

The last operation executed is the configuration of the 10-bit analog-to-digital converter. In particular, port pins RB2 and RB7 are selected as analog input respectively for the voltage and current waveforms. A specific choice of ADC configuration registers causes the ADC to automatically begin sampling a channel whenever a conversion is not active on that channel. Timer 3 acts as digitization start signal; its period, T_c, is set equal to 156.25 μs to grant a number N of points per period equal to 128. A memory register, referred to as MFLAG, mandated to retain the current state of FSM is, finally, initialized to its first value.

B. Measurement algorithms

Once the initialization phase is over, the analog-to-digital converter is enabled and the digitization of voltage, v_i, and current, i_i, waveforms starts. After an initial set of 128 samples has been acquired for both channels, a first couple of root-mean-square (RMS) values of voltage and current are available; from now on, the device evolves according to the following steps.

1. Obtained voltage RMS value is compared to three fixed thresholds respectively defining sag (RMS voltage lower than 90% of its nominal value), interruption (RMS voltage lower than 10% of its nominal value) and swell (RMS voltage greater than 110% of its nominal value).
2. If an event is detected, the state of FSM (thanks to the register MFLAG) is updated according to the recognized power quality disturbance; moreover its duration is measured.
   a. A new couple of samples are acquired and voltage and current RMS values are consequently updated; steps 1 and 2 are repeated until

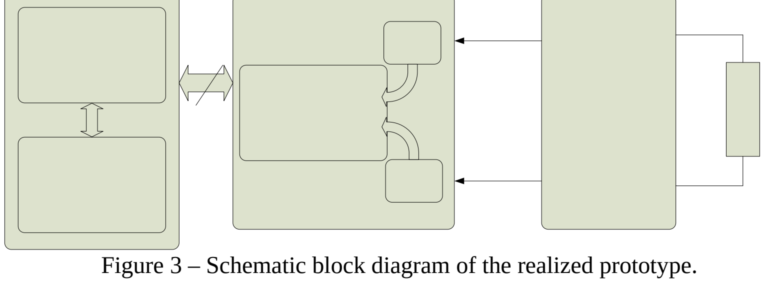

Figure 3 – Schematic block diagram of the realized prototype.

the detected event finishes.

b. When the event is over, its characteristics in terms of type and duration are sent to the storage interface for saving, thanks to a proper modification of the register MFLAG.

3. Step 1 is then repeated.

To suitably reduce the computational burden and assure real-time operations, an efficient algorithm has been adopted for RMS evaluation; in the following, the algorithm will be presented with reference to voltage samples. Similar considerations hold for current samples.

According to the traditional definition of RMS value of a discrete signal, the k^{th} value of RMS voltage V_k of the alternative component of the input voltage signal can be written as:

$$V_k = \sqrt{\frac{1}{N}\sum_{i=k}^{k+N-1}\left(v_i - \overline{v}_k\right)^2} \quad (1)$$

where $\overline{v}_k$ stands for the mean value of the acquired voltage samples $\frac{1}{N}\sum_{i=k}^{k+N-1} v_i$. For the first RMS value, equation (1) can be expressed as:

$$V_1 = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(v_i^2 + \overline{v}_1^2 - 2v_i\overline{v}_1\right)} = \sqrt{\frac{1}{N}\left(\sum_{i=1}^{N} v_i^2 - \frac{\left(N\overline{v}_1\right)^2}{N}\right)} \quad (2)$$

that can equivalently be written as:

$$NV_1^2 = \sum_{i=1}^{N} v_i^2 - \frac{\left(N\overline{v}_1\right)^2}{N} \quad . \quad (3)$$

Last expression allows a moving average technique to be adopted both on NV^2 and $\frac{\left(N\overline{v}\right)^2}{N}$, thus allowing simplifying the update of RMS value and reducing the requirement for the execution of calculations in terms of computational burden. When the $(N+1)^{th}$ sample is acquired, voltage RMS value is, in fact, updated according to the following expression (Fig. 4):

$$NV_2^2 = \sum_{i=2}^{N+1} v_i^2 - \frac{\left(N\overline{v}_2\right)^2}{N} = NV_1^2 - v_1^2 + v_{N+1}^2 - \frac{\left(N\overline{v}_1 - v_1 + v_{N+1}\right)^2}{N} \quad . \quad (4)$$

This way, a new measurement of RMS value needs only 2 additions, 3 subtractions, 3 multiplications, and a division by N; moreover, since N is a power of 2, last operation can be executed as a right shift by 7 positions (RS7) of the register containing the update of the mean value. On the contrary, if the traditional formula (1) is applied, the same results would be gathered by N subtractions, N multiplications, N-1 additions, and a division by N; the time spent for the execution of the required elementary instruction cycles would overcome the considered sampling period, thus preventing a real-time operation of the prototype. The calculations are repeated for each new acquired sample, thus assuring a closer detection of power quality events than that granted by the current recommendations (i.e. half a cycle of industrial frequency).

It is worth noting that if no event is detected, the device is programmed in such a way that it provides information about voltage THD and absorbed power. In particular, these measurements are executed every 5 seconds; an interrupt associated with Timer 5 is used to update the register MFLAG to the purpose. With regard to power, two different values, i.e. active and apparent, are evaluated by processing the digitized samples of current and voltage. In particular, apparent power is directly achieved by multiplying the obtained RMS values of voltage and current; the values are attained from those available in the DSC memory by applying an optimized root square algorithm.

Active power is evaluated according to

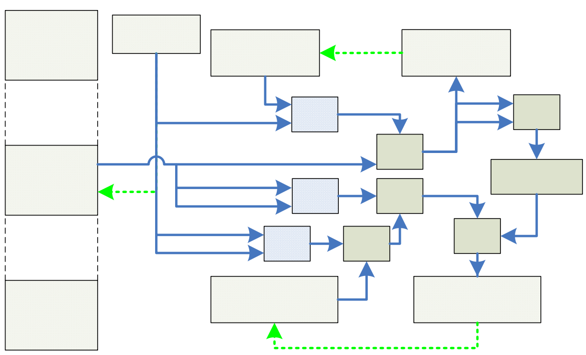

Figure 4 – Block diagram of the algorithm adopted for the effective evaluation of RSM voltage. Current values (subscript *n*) are calculated from the previous (subscript *o*) through a moving average technique and, finally, substitute them for the successive iteration (dashed line).

the expression:

$$P_{act} = \sum_{i=1}^{N} v_i i_i \qquad (5)$$

Also for this quantity, the adoption of a moving average algorithm has allowed to significantly reduce the computational burden.

To estimate voltage THD up to the 64th harmonic, a traditional discrete-time Fourier transform has been adopted on a record of 128 voltage samples. This is the reason why the memory space dedicated to voltage sample collection is large enough to contain two voltage periods; according to a traditional double-buffer implementation, while new samples are accumulated in the first buffer, the DSC applies the measurement scheme for THD to the samples already collected in the second one. Even though the code provided by Microchip for the evaluation of FFT algorithm is optimized in terms of memory occupation and execution time, it cannot be used in the considered prototype, since the time spent for the entire calculations overcome the sampling period. Due to this limitation, a modified implementation of the FFT algorithm has been exploited. In particular, FFT evaluation has been divided into 7 stages, each of which involving no more than 500 instruction cycles, thus granting to terminate the calculations before the acquisition of a new sample and meeting the conditions for real-time operations (Fig. 5). Each stage starts with an initialization phase, during which (*i*) the used registers are updated in order to continue the operations, and (*ii*) the necessary twiddle factors are evaluated.

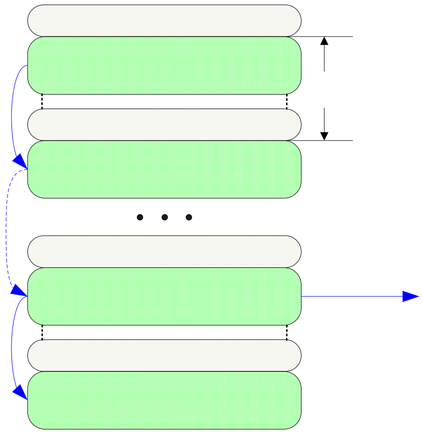

Figure 5 – Implementation of FFT used to assure real-time operations.

When the calculations related to the FFT algorithm have been terminated, the bit *THD_ready* of the register MFLAG is set. Once the digitization of the successive input samples is over, the obtained FFT coefficients are squared and used to evaluate the THD according to the following expression:

$$THD = \sqrt{\sum_{i=2}^{N} V_i^2 \Big/ V_1^2} \qquad (6)$$

where V_i^2 stands for the i^{th} squared coefficient of the FFT.

IV. EXPERIMENTAL RESULTS

A suitable measurement station has been setup with the aim of assessing the performance granted by the realized prototype. In particular, it has been realized with: (*i*) an alternate current power source AMX360 by *Pacific* (12 kVA maximum apparent power, 20 Hz-5kHz output bandwidth), (*ii*) a power meter PM100 by Voltech (5 kHz input bandwidth, maximum accuracy equal to 0.2% reading + 0.3% full range), and (*iii*) a variable resistive load (max resistance value equal to 110 Ω). The power source has remotely been controlled by mean of the corresponding module UPC-32; this way, it has been possible to generate current and voltage (either sinusoidal or affected by power quality events). The power meter has been used as reference for active and apparent power, while the durations of detected power quality events have been compared to those set in the voltage waveform generated by the power source. Different tests have been conducted on the prototype in order to investigate its capability of correctly detecting the power quality events and measuring their duration, as well as accurately providing the values of absorbed power by the resistive load in terms both of apparent and active power.

As an example, Fig. 6 shows the results obtained for measurements of apparent power for different load conditions. In particular, the evolution of results provided by the proposed device has been plotted upon the variation of nominal apparent power in the range from 337.8 to 891.5 VA; remarkable concurrence can be noticed. To further highlight the promising performance of the prototype, the measured apparent power (MPA) is compared to nominal apparent power (NPA) in Table I. Moreover, values of integral non-linearity (INL) and experimental standard deviation (σ) related to 50 independent measurements have been evaluated; values, expressed in relative percentage terms, never greater respectively than 1.0 and 0.28 have been encountered. Similar considerations hold also for power quality events; as an example, Fig. 7 shows the results obtained for measurements of sag duration. In particular, the evolution of results provided by the proposed prototype has been plotted upon the variation of nominal sag duration in the interval from 50 to 590 ms; noticeable agreement has been encountered. Finally, the measured duration (MD) is compared to nominal value (ND) in Table II.

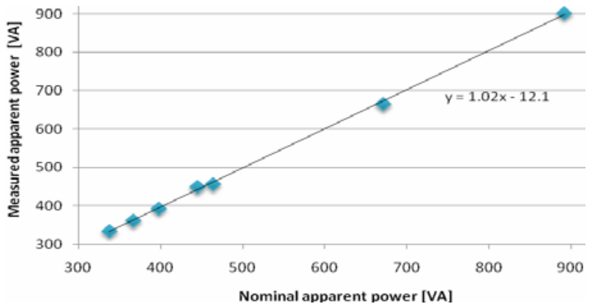

Figure 6 Evolution of the apparent power measured by the proposed prototype (blue dots) versus the nominal value obtained through the reference power meter

Table I Experimental results attained in the measurement of apparent power.

NPA [VA]	MPA [VA]	INL [%]	σ [%]
337.8	335	0.7	0.15
367.4	361	-0.3	0.16
397.6	393	-0.04	0.16
445.5	449	1.0	0.17
463.6	457	-0.8	0.12
671.1	665	-0.9	0.07
891.5	902	0.5	0.08
Max value		**1.0**	**0.28**

Values of INL and σ related to 50 independent measurements, expressed in relative percentage terms, never greater, respectively, than 0.8 and 0.15 have been attained, thus confirming the reliability of the prototype.

CONCLUSION

The paper has presented architectural details, both hardware and software, of a device prototype for electricity metering services. The core of the prototype is a microcontroller *dsPIC30F6010* by Microchip that, thanks to few spare electronic components, is capable of achieving fast and accurate of voltage and current related to a generic load. The device is mandated to identify and measure the duration of typical power quality events affecting the voltage signal provided by power distributor, as well as measure the spectral purity and the apparent and active power absorbed by a load. The performance of the prototype has been assessed by means of a suitable measurement station; obtained results have suggested the proposed prototype as a cost-effective alternative to commercial products already presented on the market.

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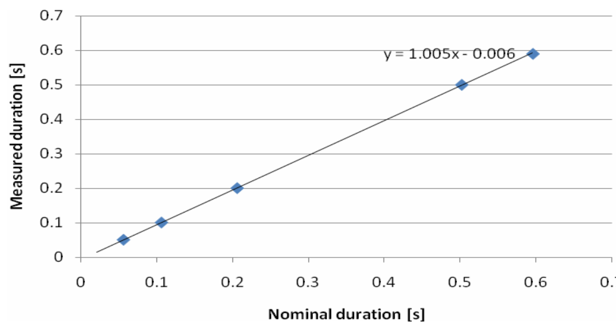

Figure 7 – Evolution of the sag duration measured by the proposed prototype (blue dots) versus the nominal value set by the power source.

Table II Experimental results attained in the measurements of sag duration.

ND [s]	MD [s]	INL [%]	σ [%]
0.050	0.056	0.5	0.15
0.100	0.106	0.5	0.08
0.200	0.206	0.6	0.06
0.500	0.501	0.8	0.02
0.590	0.595	0.6	0.01
Max value		**0.8**	**0.15**