LOGSYS Development Environment

Béla Fehér, Tamás Raikovich, Péter Laczkó

Dept. of Measurement and Information Systems, Budapest University of Technology and Economics,
Magyar Tudósok körútja 2., H-1117 Budapest, Hungary; feher@mit.bme.hu

ABSTRACT

Digital design courses are one of the basic subjects in both of the Electrical Engineering and Technical Informatics branches of BUTE. Better support for the practical experiments would help the students deeper understanding the topics and would provide good background of later more professional courses. Programmable logic devices, like FPGAs, offer a natural solution to provide real experiments with design properties of complex digital circuits and are natural choices to be a platform for system level designs. Vendor specific development tools [1] are available from the manufacturers, and these IDEs contain modules for design specification, simulation, implementation and download to evaluation boards. These demo boards are made for the demonstration of the capabilities of the actual device families and usually designed primarily for industrial and not for educational purpose. A good educational tool would support the evaluation of digital designs from the most basic experiments to medium and high level complexity through an easy-to-use application interface.

1. INTRODUCTION

The LOGSYS Development Environment [2] is a specific educational tool, which has limited capabilities, but it is very flexible for the possible application scenarios. The main goal of the development was to provide a unified environment, which manages the power, the configuration, the control and the communication tasks from a single GUI. The LOGSYS system has two main parts: the USB based development cable and the graphical user interface. A simple FPGA board has been also created, which provides direct connection to the development cable. The related materials and example designs can be downloaded from the LOGSYS webpage [3].

2. THE LOGSYS DEVELOPMENT CABLE

The development cable (see Figure 1) connects the target system with the PC through the USB port. It contains level shifter circuits, which have two reference voltage inputs: one for the configuration interface (V_{ref} JTAG) and one for the control and communication lines (V_{ref} I/O). This flexibility enables the development cable to be attached to many targets. The voltage on both reference voltage inputs can be between 1.65 V and 5 V.

JTAG TDO	JTAG TCK	CLK	MOSI	Vref I/O	5 V
JTAG TDI	JTAG TMS	RST	MISO	GND	Vref JTAG

Figure 1 The LOGSYS development cable.

A. Configuration Interface

The industry standard JTAG interface is available for design download and device configuration. This is the most widely used solution and not only for configuration but for debugging CPUs and DSPs also. The JTAG interface makes possible to use basic boundary-scan and internal signal monitoring.

B. Communication Interface

The development cable supports a range of synchronous and asynchronous serial communication protocols. The UART realizes the application level communication in case of SOPC developments. A virtual serial port driver has been created so the UART of the development cable can be accessed from Windows applications. For simple tests or educational purposes a special communication mode called BitBang I/O is available. Other supported communication modes are the USRT, the master SPI and the master I^2C.

C. Control Interface

The user can freely control the CLK clock and the RST reset lines when they are not used by other functions. In this case, the clock frequency can be set between 1 Hz and 8 MHz, and the reset signal is controlled asynchronously.

D. Power Supply and Measurement

The USB ports have short circuit protected 5 V power output and they supply enough current (500 mA) to power the development cable and smaller target systems. The development cable has a power switch with adjustable current limits of 450 mA, 700mA and 950 mA. The last two options require a Y-type USB cable. The voltage on all power lines (power output, reference voltage inputs) and the output current of the power output are measured by the cable.

3. THE LOGSYS SPARTAN-3E FPGA BOARD

An FPGA board (see Figure 2) has been created, which is simple enough for the beginners and it is also suitable for implementing more complex applications.

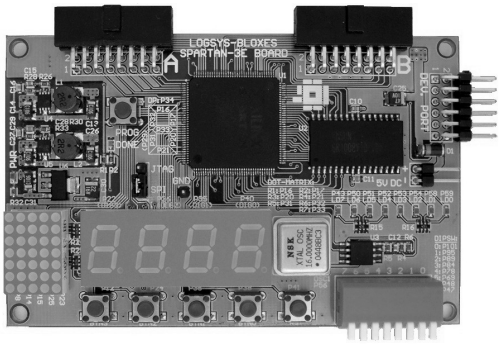

Figure 2 The LOGSYS Spartan-3E FPGA board.

The board contains a Xilinx XC3S250E-TQ144C FPGA, which enables to implement complex logic and smaller microprocessor systems. A 128 Kbyte SRAM and a 16 Mbit SPI serial Flash memory are available for storing program and data. Other on-board peripherals are one 4-digit 7-segment display, one 5x7 dot-matrix display, eight LEDs, eight switches and five push-buttons. A 16 MHz oscillator is available as a clock source. Two connectors serve for attaching different expansion modules to the board, like VGA and PS2 interface, A/D and D/A converter modules, SD card interface, etc.

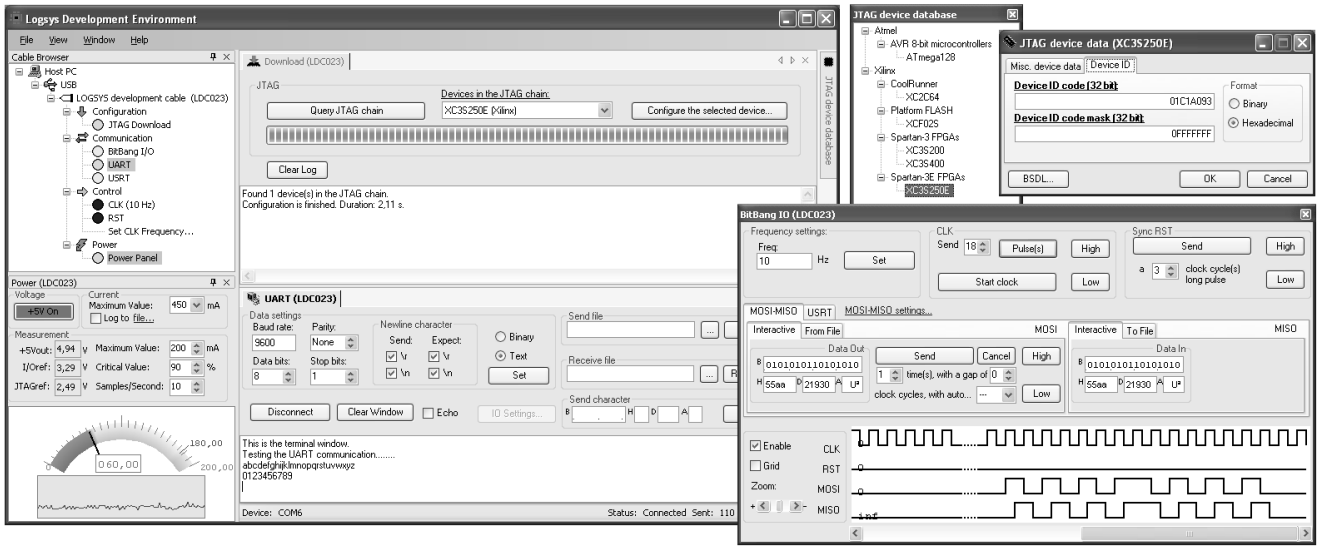

Figure 3 The LOGSYS graphical user interface.

4. THE LOGSYS USER INTERFACE

The user application has a customizable and well-arranged graphical user interface (see Figure 3) for accessing functions provided by the development cable. The graphical user interface is implemented using docking windows. Every function has its own graphical interface and they are displayed in separate child windows.

A. Cable Browser and Power Panel

The cable browser displays the connected development cables and the available functions on each cable. A function can be enabled by double-clicking on its name. Functions that require the same resources cannot be enabled at the same time. The user can control the power output and the output current limit from the power panel. This interface also serves for displaying the measurement results and the history of the power consumption.

B. JTAG Configuration

The LOGSYS system uses the industry standard SVF file format [4] to describe the operations on the JTAG chain. Most manufacturer tools provide a way to create an SVF file that contains the configuration data. In case of Xilinx devices, the BIT and the JEDEC formats are also supported by invoking the manufacturer's iMPACT application [1]. The LOGSYS configuration tool has an internal device database to manage devices from different manufacturers in the JTAG chain. The required data can be entered manually or can be imported from BSDL files of the devices. Using the JTAG device database, composite JTAG chains containing devices from different vendors can be handled also without problems. At the beginning of the configuration process, the devices in the JTAG chain have to be queried first. Then the user can download the configuration file to the selected device.

C. BitBang I/O

The BitBang I/O is a special low-speed synchronous communication mode for simple tests and educational purposes. In this mode, the software directly controls the CLK clock, changes the RST reset and the MOSI serial data out lines, and samples the MISO data input at the rising or falling clock edge. The clock frequency can be set between 1 Hz and 1000 Hz. The clock can be in free run mode or the user can send a given number of clock pulses. When the clock is stopped the commands are queued, and they going to be executed after the clock is restarted. The reset signal can be set to low or high, also a reset pulse with a given length can be sent. Manual or file I/O operations are supported. A timing diagram is available that displays the communication flow. The BitBang I/O feature allows the step-by-step analysis of the tested logic, and it is important in case of state machines and simple functional units.

D. UART/USRT Terminal

A simple terminal interface is available for UART and USRT communication. The user can adjust various parameters like the baud rate, the number of start and stop bits, the parity and the newline characters. The terminal interface supports binary and text mode communication, as well as file I/O operations. In USRT mode, the development cable drives the clock output and the clock frequency is equal with the baud rate.

5. AN EXAMPLE DESIGN

Creating a simple calculator (see Figure 4) is one of the exercises for the students at Embedded and Ambient Systems Laboratory held by our department. With the free ISE WebPack software [1] and the LOGSYS tool, the students can easily implement and test such designs.

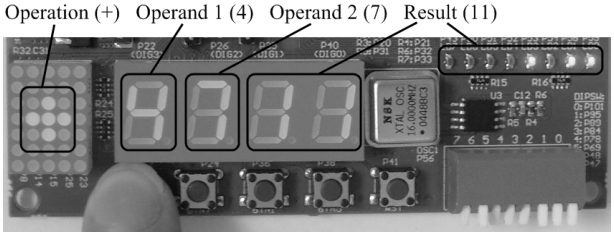

Figure 4 The simple calculator.

REFERENCES

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http://www.xilinx.com/ise/logic_design_prod/webpack.htm

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[3] LOGSYS webpage http://logsys.mit.bme.hu

[4] Serial Vector Format Specification, ASSET InterTech, Inc.
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