AN EFFICIENT $\Delta\Sigma$ NOISE-SHAPING ARCHITECTURE

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I. Introduction

$\Delta\Sigma$ analog-to-digital converters are capable of achieving high resolution in wideband applications. Often these designs use multi-stage structure with small oversampling ratio (OSR[1]), incorporating multibit quantizers. One example is the Leslie-Singh architecture which requires a multibit quantizer in the second stage, clocked by the oversampling clock (Fig. 1(a)). Because only very fast ADC's can meet this requirement, it is advantageous to use a reduced-sample-rate second stage, as suggested in [1] (Fig. 1(b)).

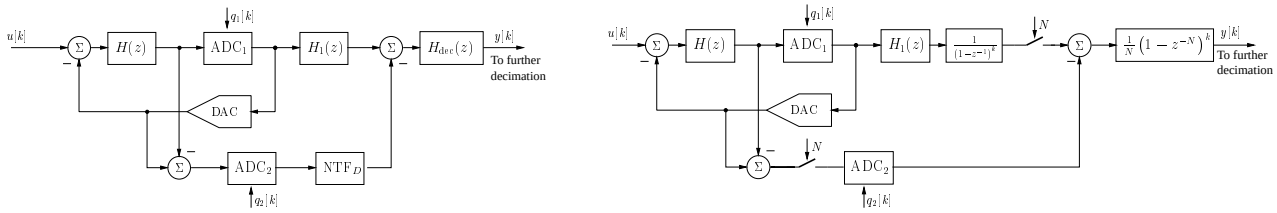

Figure 1: (a) The Leslie-Singh and (b) the reduced-sample-rate architecture

This structure is based on the observation that an N^{th}-order noise transfer function (NTF) is similar to the denominator of the same order decimation filter, if the filter is the traditional "sinc-type" filter. In this case the denominator of the sinc filter cancels the digital NTF following the multi-bit ADC, and one can reduce the clock frequency of the second stage by N. Unfortunately, it also causes an N-fold increase in the noise power [2]. This means that the signal to (inband) noise ratio (SNR) decreases by 3 dB for each doubling of N.

In the following, an optimizing technique is introduced which can avoid this SNR loss.

II. Optimized transfer function

In the ideal case, the output of a two-stage modulator contains only the input signal and the quantization noise of the second stage, i.e. $Y = H_1 H_{\rm dec} U + H_2 H_{\rm dec} Q_2$ (Fig. 1), where H_1 is usually a delay factor, H_2 is the digital replica of the first-stage noise transfer function, and $H_{\rm dec}$ is the transfer function of the decimation filter. In order to use the reduced-sample-rate architecture, H_2 should be cancelled by the denominator of $H_{\rm dec}$. In this case, Y becomes

$$Y = H_1 H_{\rm dec} U + {\rm num}(H_{\rm dec}) Q_2 . \tag{1}$$

In order to maximize the SNR, the power of the inband noise should be minimized. This can be done by modifying the zeros of $H_{\rm dec}$. The poles of $H_{\rm dec}$ should be chosen so as to cancel the zeros around $f = 0$, and hence the NTF of the first stage should be modified as well in order to be cancelled by the denominator of the decimation filter.

[1] In the terminology of $\Delta\Sigma$-converters, OSR is the ratio of the samping rate of the modulator (f_s) and the Nyqist rate of the signal ($2f_{\rm bw}$).

Assuming that the decimation ratio of the first decimation stage is N, a second-order $H_{\rm dec}$ and the NTF with the modified zeros and poles can be described as

$$H_{\rm dec}(z) = \frac{1 - 2(\cos N\alpha)z^{-N} + z^{-2N}}{1 - 2(\cos\alpha)z^{-1} + z^{-2}},\ NTF = 1 - 2(\cos\alpha)z^{-1} + z^{-2} \tag{2}$$

where α represents the angle of the complex conjugate zeros. If $\alpha \neq 0$, $H_{\rm dec}(z)$ becomes the so-called Rotated Sinc (RS) filter [3]. In our case α should be optimized to minimize the inband noise power of Q_2, i.e. to minimize

$$\int_0^{\frac{f_s}{2\,OSR}} |{\rm num}(H_{\rm dec})|^2\, df. \tag{3}$$

Substituting ${\rm num}(H_{\rm dec})$ into Eq. (3), the optimal α in our case becomes

$$\alpha = \frac{1}{N}\cos^{-1}\left(\frac{\sin\left(\frac{\pi N}{OSR}\right)}{\frac{\pi N}{OSR}}\right). \tag{4}$$

In a second-order structure one can achieve 3.8 dB improvement in the SNR using this method as compared to the traditional NTF and sinc filter.

III. Result, Conclusion

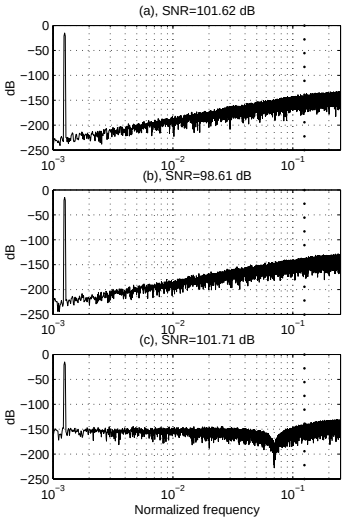

Figure 2: The output spectra.

The introduced technique has been validated using MATLAB simulation of a second-order Leslie-Singh structure with an oversampling ratio of 4. The output spectrum and the SNR after the first decimation stage are shown in Fig. 2. The dotted lines show the boundary of the signal band.

Fig. 2(a) shows a 2nd order modulator with full-speed second stage and 3rd order decimator (original structure), Fig. 2(b) shows the reduced-sample-rate architecture with 2nd order decimation, and Fig. 2(c) shows the proposed architecture with 2nd order decimation. The inband noise power has been reduced by more than 3 dB in this latter one compared to the reduced-sample-rate structure, so there is no loss in SNR compared to the original full-speed structure.

The introduced method can be extended also for higher-order modulators. It can be shown that the SNR achieved by the proposed design is then even better than that of the original full-speed structure. The described method is an optimization of the complete MASH structure, hence, it gives different results than the simple optimization of the zeros of a single-stage modulator [4] or the zeros of the decimation filter itself [3].

References

[1] Wei Qin, Bo Hu, and Xieting Ling. "Sigma-delta ADC with reduced sample rate multibit quantizer". *IEEE Trans. on Circuits and Systems – II. Analog and Digital Signal Processing*, 46(6):824–828, June 1999.

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