Digital design lab 4B
Digital design lab 4B

• Outline:
  • SR latch
  • 8-bit register
  • D flip-flop
  • Counter with D flip-flops
Digital design lab 4B

- SR-latch: cross-coupled NOR gates
- Recall:
  - $S=1$, $R=0$: $Q=1$
  - $S=0$, $R=1$: $Q=0$
  - $S=0$, $R=0$: $Q$ holds its value
  - $S=1$, $R=1$: oscillation!
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• Launch Xilinx ISE

• Create new project
Digital design lab 4B

• Name: Digital_design_lab_4B
• Work on drive D:
• Press Next
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• Verify settings:
  • Family
  • Device
  • Package
  • Speed

• Press Next
• Press Finish
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• Right click on the label, and select New Source...
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- Select Verilog module
- Name: SR_latch
- Do not modify Location
- Check “Add to project”
- Press Next
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- Leave the table blank, press Next, then Finish
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- Add the following source code
- #10 after the assign introduces some delay to simulate the behavior of real gates

```verilog
module SR_latch(
    input S,
    input R,
    output Q,
    output Q_n
);

assign #10 Q = ~R|Q_n;
assign #10 Q_n = ~(S|Q);

endmodule
```

- Press Save
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- Switch to simulation mode

- Right click on the label, and select New Source...
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- Select Verilog Test Fixture
- Do not modify Location
- Check “Add to project”
- Press Next
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• Select SR_latch on the next window, and press Next, then press Finish
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• Add the following code after the “Add stimulus here” part

```c
// Add stimulus here
#100; S = 1; R = 0;
#100; S = 0; R = 0;
#100; S = 0; R = 1;
#100; S = 0; R = 0;
#100; S = 1; R = 1;
#100; S = 0; R = 0;
```

• Press Save
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• Left click on the test fixture file

• Then open the submenu under “Isim Simulator”, right click on “Simulate Behavioral model”, and select “Rerun all”
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• Press the Zoom to full view button

• Study the waveforms:

• Study the effect of the Set, Reset inputs on Q, and the effect of switching from SR=11 to SR=00.

• Close the simulator
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• Registers:

  • **Register**: multiple flip-flops sharing clock signal
    
    - From this point, we’ll use registers for bit storage
    
    • No need to think of latches or flip-flops
    
    • But now you know what’s inside a register
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• Switch back to implementation mode

• Right click on the label and select New Source
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- Name: Register_8
- Don’t modify Location
- Check Add to project
- Press Next
Digital design lab 4B

- Leave the table blank, press Next, then press Finish
Digital design lab 4B

• Add the following code

```verbatim
module Register_8(
  input [7:0] I,
  input clk,
  output reg [7:0] Q
);

always @ (posedge clk)
  Q <= I;

endmodule
```

• Press Save
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• Right click on the label, and select New Source
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• Select Verilog Module
• Name: Top
• Don’t modify Location
• Check “Add to project”
• Press Next
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- Leave the table blank, press Next, then press Finish
Digital design lab 4B

- Add the following source to the Top module:

```plaintext
module Top(
    input [0:0] bt,
    input [7:0] sw,
    output [7:0] ld
);

Register_8 Reg8(.I(sw[7:0]), .clk(bt[0]), .Q(ld[7:0]));

endmodule
```

- Press Save
Now we will implement and download the module to the FPGA board. A file has been prepared for this purpose, you can download it using the following link: [download]

If the browser opens the file instead of displaying the download dialog window: right click, and select “Save as…”

Download the file, and save it to the **current working directory** of your project (D:\Digital_design_lab_4B).

If you are not sure, you can check it in the title bar of the ISE (top of the ISE window)
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• Go back to the ISE, right click on the „xc3s250e-4tq144” label and select „Add copy of source”
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• Browse the file you have downloaded, select it and press Open:
The following window appears:

Press OK

If you have difficulties, ask for assistance
Digital design lab 4B

• Now open the previously added file. Uncomment the bt<0> signal first: select the line, right click and select Uncomment-> Line(s)

```plaintext
16  # 4 darab aktív magas nyomógomb, balról jobbra sz.
17  #NET "bt<3>"  LOC = "P12";
18  #NET "bt<2>"  LOC = "P24";
19  #NET "bt<1>"  LOC = "P36";
20  #NET "bt<0>"  LOC = "P38";
21
22  # 8 kapcsoló, balról jobbra
23  #NET "sw<7>"  LOC = "P47";
24  #NET "sw<6>"  LOC = "P48";
25  #NET "sw<5>"  LOC = "P69";
26  #NET "sw<4>"  LOC = "P78";
27  #NET "sw<3>"  LOC = "P84";
```
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- In addition, add the following setting to the end of line in order to use bt<0> as a clock signal:
  | CLOCK_DEDICATED_ROUTE = FALSE;

19  #NET  "bt<1>"  LOC  =  "P36";
20  NET  "bt<0>"  LOC  =  "P38"  |  CLOCK_DEDICATED_ROUTE  =  FALSE;
• Uncomment the sw inputs:

```plaintext
22  # 8 kapcsoló, balról jobbra számozva
23  #NET "sw<7>"  LOC = "P47";
24  #NET "sw<6>"  LOC = "P48";
25  #NET "sw<5>"  LOC = "P69";
26  #NET "sw<4>"  LOC = "P79";
27  #NET "sw<3>"  LOC = "P99";
28  #NET "sw<2>"  LOC = "P89";
29  #NET "sw<1>"  LOC = "P79";
30  #NET "sw<0>"  LOC = "P69"
31
32  # 8 LED, balról jobbra
33  #NET "ld<7>"  LOC = "P47"
```
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• Uncomment the ld signals:

32  # 8 LED, balról jobbra számozva
33  #NET "ld<7>"
34  #NET "ld<6>"
35  #NET "ld<5>"
36  #NET "ld<4>"
37  #NET "ld<3>"
38  #NET "ld<2>"
39  #NET "ld<1>"
40  #NET "ld<0>"

• Press Save
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• Left click on the Top module

• Then right click on “Generate Programming File”, and select “Rerun All”
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• You will see the following warning after the generation: “A clock IOB / clock component pair have been found that are not placed at an optimal clock IOB / clock site pair. ....”

• You can ignore this one, in case of any other errors or warnings, ask for assistance.
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• If the program file was generated successfully, you can connect the FPGA board to the PC

• Mind the orientation of the JTAG connector!
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• Launch the Logsys GUI application

• Press the +5V button to turn the board on
Digital design lab 4A

• On the right side of the screen, select JTAG download:

• Press the „Query JTAG chain” button

• Then press „Configure the Selected Device”
Digital design lab 4B

• Browse the generated file in your working directory

• Press Open
Digital design lab 4B

• Now set some random input combinations on the switches, and press the BT0 button for the rising edges on the clock input of the register.
• The input should appear on the LEDs after the rising edges.
Digital design lab 4B

- Up-counter with D flip-flops:
Digital design lab 4B

• Open the ISE, right click on the label and select New Source...
Digital design lab 4B

- Name: D_FF
- Don’t modify Location
- Check “Add to project”
- Press Next
Digital design lab 4B

- Leave the table blank, press Next, then press Finish
Digital design lab 4B

• Add the following code to the module

```verilog
define module D_FF(
  input D,
  input clk,
  output reg Q,
  output reg Q_n)

  always @(posedge clk)
  begin
    Q <= D;
    Q_n <= ~D;
  end
endmodule
```

• Press Save
Digital design lab 4B

• Open the Top module, delete the Reg8 register
• Modify the inputs and outputs of the module: add clk, remove the switches and bt[0:0]:

```
module Top(
  input clk,
  output [7:0] ld
);
```
Digital design lab 4B

- Add the following source to the module:

```verbatim
module Top(
    input clk,
    output [7:0] ld
);
wire Qn0, Qn1, Qn2, Qn3; // wires connected to the Q_n outputs of the Flip-flops
D_FF D0(.D(Qn0), .clk(clk), .Q(ld[0]), .Q_n(Qn0));
D_FF D1(.D(Qn1), .clk(Qn0), .Q(ld[1]), .Q_n(Qn1));
D_FF D2(.D(Qn2), .clk(Qn1), .Q(ld[2]), .Q_n(Qn2));
D_FF D3(.D(Qn3), .clk(Qn2), .Q(ld[3]), .Q_n(Qn3));
assign ld[7:4] = 4'h0;
endmodule
```

- Press Save
Digital design lab 4B

- Open the LOGSYS_SP3E.ucf file
- Comment the \texttt{bt<0>} and \texttt{sw} lines by inserting a \# character to the beginning of each line:

```plaintext
21  \#NET "bt<0>" CLOCK_DEDICATED_ROUTE = FALSE;
22
23  \# 8 kapcsoló, balról jobbra számozva
24  \#NET "sw<7>" LOC = "P47";
25  \#NET "sw<6>" LOC = "P48";
26  \#NET "sw<5>" LOC = "P69";
27  \#NET "sw<4>" LOC = "P78";
28  \#NET "sw<3>" LOC = "P84";
29  \#NET "sw<2>" LOC = "P89";
30  \#NET "sw<1>" LOC = "P95";
31  \#NET "sw<0>" LOC = "P101";
```
Digital design lab 4B

• Uncomment the clk signal at the beginning of the file

```vhdl
10  # LOGSYS Fejlesztőkábel GUI vezérlő és kommunikációs jelek
11  #NET "mosi"   LOC = "P120";
12  #NET "miso"   LOC = "P143";
13  NET "clk"     LOC = "P129" | PULLDOWN;
14  #NET "rst"    LOC = "P119" | PULLDOWN;
```

• Press Save
Digital design lab 4B

• Regenerate the programming file, and upload the new binary to the FPGA board
• Now the circuit requires to add a system clock input for the circuit
• First set the value of the clock frequency to 1 Hz
• Press the Set button
• Click into the CLK checkbox
• Note: on Windows 10 the tick might not appear, but it should be fine
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• You should see the counter counting up, 1/sec.
• If you want to increase the speed of the counter, modify the clock frequency.
• The counter can count up to 15. Try to increase the maximum value to 255. How many bits do you need in order to reach 255?
• Hint: What is the relation between the maximum value and the number of D flip-flops?