Digital Design first homework

Deadline: November 3, 2019

Admission: a PDF file, sent to lecturer: palfi@mit.bme.hu. You can submit your work anytime before the deadline. The e-mail should contain the pdf file, your name, Neptun code and personal code (see later).
Format: all work should be done electronically (Word, LibreOffice Writer, LaTeX, etc.).
Contents: **Please give detailed information about the process of the design work. Final results without appropriate reasoning will be rejected**.
As you are going to be an engineer, we require a clean, tidy work. **Untidy, illegible works will also be rejected.**
Task: Design a synchronous 3-bit sequence generator, which presents its possible 8 states on its output in a prescribed order. The order is specified by the digits of your personal homework code (given by the lecturer), extended by a 0 digit at the start. You are going to implement it with 3 different methods:

Task 1: Design a finite state machine (FSM) (using a 3-bit register with synchronous reset input) that directly generates the repeating sequence of numbers defined by your personal code.
For example, if the personal code is 7312546, then the state transitions should start from 0, then step to 7, to 3, to 1, to 2, to 5, to 4, to 6 and back to 0, according to the requirements.
Also, create the Verilog HDL description of the system and verify the design with simulation.
Following should be submitted with your comments and explanations:
- State diagram and state table
- Truth table for the combinational logic
- Canonical form and simplified form
- Verilog source and simulation output

Task 2: „If something can be done mechanically, the computer should do it”: from the state diagram the design process can be done by the computer. Instead of manually generating the truth table and the state diagram, etc., we can just describe it in Verilog, with *always @(*)* and *case... endcase* statements.
- Implement the design without manually generating the Boolean functions, using *always @(*)* and *case… endcase*
- In the submission you should include the Verilog source and the output of the simulation.