

Fig. 4. Nets in the proof of Theorem 2.

Deciding whether a graph $G = (V, E)$ is bipartite is equivalent to finding a two-coloring for the vertices of G . This can be done in $O(|V| + |E|)$ time by using depth first search [6]. Furthermore, it is impossible to decide whether a general graph is bipartite in time less than the number of edges in the graph. Notice that the number of edges in an interaction graph of a given channel routing problem with n nets can be as large as $O(n^2)$. Fig. 3 shows an example of such a case. Nevertheless, we would like to have an algorithm that recognizes if a channel routing problem admits an internal-external layout in $O(n)$ time.

Using Lemmas 1 and 2, it is easy to prove that the following is equivalent to Theorem 1.

Corollary 1: Let P be a given channel routing problem. P admits an internal-external layout if and only if it can be decomposed into two (channel routing) subproblems P_A and P_B such that both P_A and P_B are river routing problems. \square

Next, we will present a greedy algorithm that decides whether a given channel routing problem P admits an internal-external layout. If the answer is positive it decomposes P into two subproblems P_A and P_B such that both P_A and P_B are river routing problems.

Algorithm DECOMPOSE

- (1) Let N_0 be a fictitious net whose terminals are to the left of the leftmost terminals on each shore.
- (2) Set $front(A) := N_0$; and $front(B) := N_0$.
- (3) Scan the terminals on the bottom shore from left to right:
 - for** every bottom terminal b_i encountered **do**
 - if** N_i interacts with $front(A)$ **then**
 - if** N_i does not interact with $front(B)$ **then**
 - put N_i in set B and set $front(B) := N_i$
 - else**
 - print ("the problem does not admit an internal-external layout"); **stop**
 - end-if**
 - else**
 - put N_i in set A and set $front(A) := N_i$
 - end-if**
 - end-for.** \square

Theorem 2: Let P be a given channel routing problem with n nets. Algorithm DECOMPOSE decides if P can be decomposed into two subproblems P_A and P_B such that both P_A and P_B are river routing problems, and if the answer is yes, it computes such a decomposition. Its time complexity is $O(n)$.

Proof: Suppose that the algorithm decides that P cannot be decomposed as discussed above. Then there is a net N_j such that N_j interacts with $front(A) = N_a$ and $front(B) = N_d$ (i.e., $t_j < t_a$ and $t_j < t_d$). Let N_c be the net that is $front(A)$ when net N_d is encountered ($a = c$ is possible). Net N_c belongs to the set A and interacts with net N_d (i.e., $t_d < t_c$). Hence, $t_j < t_d < t_c$. Furthermore, because of the order in which nets are processed, $b_c < b_d < b_j$. This implies that net N_j interacts with nets N_d and N_c , see Fig. 4. Hence, nets N_j , N_c , and N_d interact pairwise. Therefore, P cannot be decomposed into two subproblems P_A and P_B such

that both P_A and P_B are river routing problems. Clearly, if the algorithm succeeds, then P can be decomposed as stated in the theorem.

At each iteration of the **for** loop, the algorithm spends constant time. Hence, its time complexity is proportional to the number of iterations, which is n . \square

Notice that algorithm DECOMPOSE needs only a constant amount of extra storage.

REFERENCES

- [1] J. R. S. Blair and E. L. Lloyd, "Generalized River Routing—Algorithms and performance bounds," Lecture Notes in Computer Science: VLSI Algorithms and Architectures (*Proc. AWOC '86*), vol. 227, pp. 317–328, Springer-Verlag, 1986.
- [2] C. E. Leiserson and R. Y. Pinter, "Optimal placement for river routing," *SIAM J. Computing*, vol. 12, no. 3, pp. 447–462, 1983.
- [3] E. L. Lloyd and S. S. Ravi, "One-layer routing without component constraints," *J. Computer and Syst. Sci.*, vol. 28, no. 3, pp. 420–438, 1984.
- [4] A. Mirzaian, "Channel routing in VLSI," in *Proc. STOC '84*, pp. 101–107, 1984.
- [5] F. P. Preparata and W. Lipski, Jr., "Optimal three-layer channel routing," *IEEE Trans. Computers*, vol. 33, pp. 427–437, 1984.
- [6] E. M. Reingold, J. Nievergelt, and N. Deo, *Combinatorial Algorithms*. Englewood Cliffs, NJ: Prentice-Hall, 1977.
- [7] R. L. Rivest and C. M. Fiduccia, "A 'greedy' channel router," in *Proc. 19th Design Automation Conf.*, pp. 418–424, 1982.
- [8] T. Yoshimura and E. Kuh, "Efficient algorithms for channel routing," *IEEE Trans. Computer-Aided Design*, vol. CAD-1, pp. 25–35, 1982.

Resonator-Based Digital Filters

GÁBOR PÉCELI

Abstract—This paper presents a digital filter structure that is both structurally passive and can suppress all zero-input limit cycles, and if rounding is applied provides minimum roundoff noise. These properties are due to the fact that this structure generates its output as a linear combination of orthogonal signal components, thus internally implementing an orthogonal realization of a lossless transfer function.

I. INTRODUCTION

Recently a common structure for recursive discrete transforms has been derived [1] that is based on the state-variable formulation and the results of the observer theory [2]. By applying a generalization of the "frequency sampling" method [3], this structure can be efficiently used also to FIR and IIR filtering operations. The block diagram of the transformer structure is given in Fig. 1. This structure consists of digital resonators embedded into a common feedback loop. Due to this feedback, the properties of this structure substantially differ from that of the well-known "frequency sampling" structures [3]. In this paper it is shown that using this approach digital filters can be derived that are structurally passive, suppress all zero-input limit cycles, and if rounding is applied provide minimum roundoff noise. Having these properties it can be stated that the proposed structure is a real alternative of the best structures known from the literature, like the wave digital filters [4], orthogonal filters [5], and the filters based on the lossless bounded real (LBR) two-pair extraction [6].

Manuscript received March 29, 1988.

The author is with the Department of Measurement and Instrument Engineering, Technical University of Budapest, H-1521 Budapest, Hungary.
IEEE Log Number 8824473.

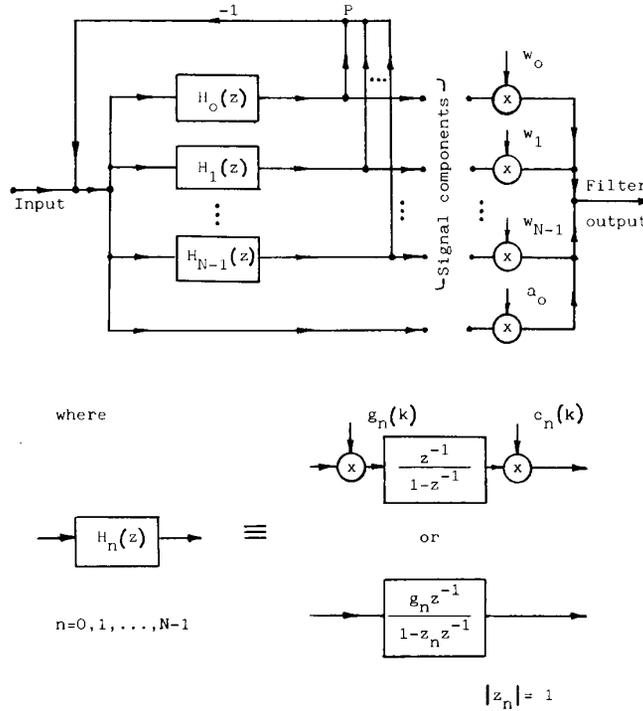


Fig. 1. The suggested common structure for recursive transformations.

II. PROPERTIES OF THE SUGGESTED STRUCTURE

In this letter we will concentrate on the time-invariant version of the common transformer structure (see Fig. 1), and for simplicity we do not consider the case of multiple resonator poles. Without loss of generality, starting from the usual form of single-input single-output digital transfer functions (having real coefficients)

$$H(z) = \frac{\sum_{n=0}^{N-1} a_n z^{-n}}{1 + \sum_{n=1}^{N-1} b_n z^{-n}} = a_0 + H'(z) \tag{1}$$

we will consider only the implementation of $H'(z)$, which using the notations of Fig. 1, can be written in the following form

$$H'(z) = \frac{\sum_{n=0}^{N-1} \frac{g_n z^{-1}}{1 - z_n z^{-1}} w_n}{1 + \sum_{n=0}^{N-1} \frac{g_n z^{-1}}{1 - z_n z^{-1}}} \tag{2}$$

where $|z_n|=1$, $w_n = H'(z_n)$, $n=0,1,\dots,N-1$, and if $p_n(n=0,1,\dots,N-1)$ are the poles of $H'(z)$,

$$g_n = z_n \frac{\prod_{m=0}^{N-1} (1 - p_m z_n^{-1})}{\prod_{m=0, m \neq n}^{N-1} (1 - z_m z_n^{-1})}, \quad n=0,1,\dots,N-1. \tag{3}$$

The internal part of this structure, which realizes the recursive part of the transfer function, can be characterized by the transfer

function from the input to point P (see Fig. 1):

$$H_p(z) = \frac{\sum_{n=0}^{N-1} \frac{g_n z^{-1}}{1 - z_n z^{-1}}}{1 + \sum_{n=0}^{N-1} \frac{g_n z^{-1}}{1 - z_n z^{-1}}} \tag{4}$$

It is easy to show that $H_p(z)$ is the transfer function of an all-pass filter (i.e., it is lossless), if $g_n = r_n z_n$, $n=0,1,\dots,N-1$, where $\{r_n\}$ are (for stable transfer functions positive) real numbers, and

$$\sum_{n=0}^{N-1} r_n = 1 \tag{5}$$

see [7]. At this point it worth developing a link to the usual state variable formulation. For simplicity we will use the "complex version" of the state equations

$$\begin{aligned} x(n+1) &= (F - GC)x(n) + Gu(n) = Ax(n) + Bu(n) \\ y(n) &= Cx(n) + Du(n) \end{aligned} \tag{6}$$

where $x(n)$ is an N -dimensional vector describing the state of the system, $u(n)$ is the scalar input, $y(n)$ is the scalar output, while F , A , G , B , and C are, respectively, $N \times N$, $N \times N$, $N \times 1$, $N \times 1$ and $1 \times N$ constant matrices. $D=0$ in our case, and $F = \text{diag}(z_0, z_1, \dots, z_{N-1})$, $G^T = [g_0, g_1, \dots, g_{N-1}] = R^T F$, where $R^T = [r_0, r_1, \dots, r_{N-1}]$.

The LBR lemma [8] states that $H'(z)$ is LBR if and only if for the minimal realization $\{A, B, C, D\}$ there exists a positive definite matrix P such that

$$\begin{aligned} A^*PA + C^*C &= P \\ B^*PB + D^*D &= I \\ A^*PB + C^*D &= 0 \end{aligned} \tag{7}$$

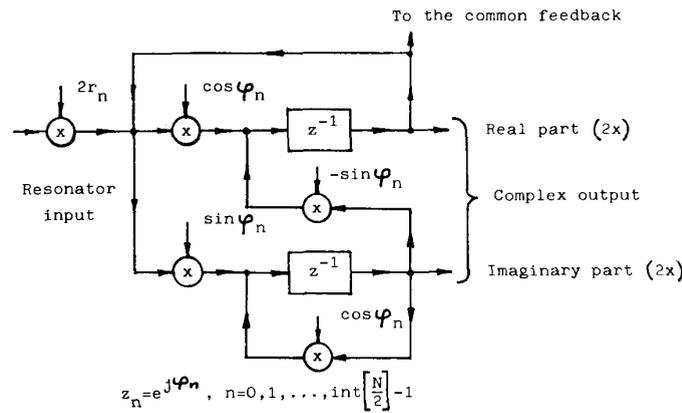


Fig. 2. A possible second-order resonator block for the common structure.

where the superscript $*$ denotes conjugate transposition. P is the observability Grammian [9]:

$$P = \sum_{k=0}^{\infty} A^{k*} C^* C A^k \quad (8)$$

which for our case has the form of

$$P = \text{diag} \langle r_0^{-1}, r_1^{-1}, \dots, r_{N-1}^{-1} \rangle. \quad (9)$$

Thus we have a "non-scaled" orthogonal realization, the scaling (which results in $P = I$) affects only the elements of R and C .

Vaidyanathan and Liu proved [10], that if $Q - A^*QA$ is positive semidefinite for some diagonal matrix Q of positive elements, then all zero-input limit cycles can be suppressed. For our case $Q = P = \text{diag} \langle r_0^{-1}, r_1^{-1}, \dots, r_{N-1}^{-1} \rangle$ is the proper choice to fulfil this condition. The proof is straightforward: the eigenvalues of $Q - A^*QA$ are all zero except one, which is positive. Thus if the unavoidable quantizers ($Q[x]$) are such that each state variable is quantized independently of others, quantization is performed in front of the delay elements, and magnitude-truncation strategy is applied when $-1 \leq x < 1$, and 2's-complement overflow operation when x exceeds this range, then there are no self-sustained zero-input oscillations of either type (roundoff or overflow) in the proposed structure.

Mullis and Roberts [11] investigated the conditions of minimum roundoff noise in fixed-point digital filters. They found that if the

$$\begin{aligned} K &= AKA^* + BB^* \\ W &= A^*WA + C^*C \end{aligned} \quad (10)$$

matrices are simultaneously diagonal, then, if we adopt their model, we have an optimal realization considering roundoff noise effects. In our case

$$K = \text{diag} \langle r_0, r_1, \dots, r_{N-1} \rangle = IR \quad (11)$$

$$W = \text{diag} \langle r_0, r_1, \dots, r_{N-1} \rangle = P = Q \quad (12)$$

thus the proposed structure is optimal even in this sense.

III. FILTER DESIGN AND IMPLEMENTATION

If (5) holds, $H_p(z)$ implements an all-pass filter, and if so, we know even its zeros, since they are in mirror image relationship with the poles of $H'(z)$. This property is the key to the determination of those resonator positions which will provide the above properties. These positions coincide with the zeros of $1 - H_p(z)$ [7]. We will have two sets of resonator poles, since the filter poles do not specify the sign of $H_p(z)$. The number of nonzero filter

poles should be at least one less than that of the resonator poles, since $H_p(z)$ is forced to have at least one zero at the origin, otherwise the loop would be delay free. Thus the filter design consists of the following steps.

1) Find the proper transfer function $H'(z)$ having not more than $N-1$ nonzero poles and zeros. (According to (1), $H'(z)$ has a zero at the origin, which can be easily eliminated by modifying the tap connections in Fig. 1, if necessary.)

2) Find the transfer function $H_p(z)$ from the poles of $H'(z)$, and determine the resonator pole positions from the zeros of $1 - H_p(z)$. Note that $H_p(z)$ should have at least one zero at the origin, and there are two sets of resonator poles.

3) Find the r_n , $n=0,1,\dots,N-1$, (positive real) values

$$r_n = \frac{\prod_{m=0}^{N-2} 1 - p_m z_n^{-1}}{\prod_{\substack{m=0 \\ m \neq n}}^{N-1} 1 - z_m z_n^{-1}}, \quad n=0,1,\dots,N-1 \quad (13)$$

[see (3)]. Note that two sets of r_n values will be available.

4) Find the two sets of w_n , $n=0,1,\dots,N-1$, (typically complex) values

$$w_n = H'(z_n). \quad (14)$$

5) Select one of the parameter sets for realization. The practical implementation requires for real resonator poles first order, and, for complex resonator poles, second-order sections. The block diagram of a possible alternative for this latter is given in Fig. 2. Other structures that preserve the "internal orthogonality," like the different versions of the coupled-form [12], are also suitable. For such resonator blocks all the properties discussed in Section II remain valid, only the matrices will have a slightly different form.

IV. CONCLUSIONS

In this paper a resonator-based structure has been investigated, which seems to be suitable to form a (possibly VLSI implemented) common base for every linear filtering-like signal processing operation. The proposed structure can be applied in a wide variety of forms. One form is the direct utilization of the common structure (see Figs. 1 and 2). An alternative utilization can be the implementation of those filters which are based on parallel connection of two all-pass filters [13]. Obviously simple first- and second-order building blocks can also be derived, and the realization of adaptive filters can also be considered. All these

versions are of practical interest, since at the price of some redundancy, all of them provide efficient realizations concerning sensitivity, stability and roundoff noise.

REFERENCES

- [1] G. Péceli, "A common structure for recursive discrete transforms," *IEEE Trans. Circuits Syst.*, vol. CAS-33, pp. 1035-1036, Oct. 1986.
- [2] G. H. Hostetter, "Recursive discrete Fourier transformation," *IEEE Trans. Acoustics, Speech, Signal Processing*, vol. ASSP-28, pp. 183-190, Apr. 1980.
- [3] L. R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1975, p. 47.
- [4] A. Fettweis, "Wave digital filters: Theory and practice," *Proc. IEEE*, vol. 74, pp. 270-327, Feb. 1986.
- [5] P. Dewilde and E. Deprettere, "Orthogonal cascade realization of real multipoint digital filters," *Int. J. Circuit Theory Appl.*, vol. 8, pp. 245-277, 1980.
- [6] P. P. Vaidyanathan, "A unified approach to orthogonal digital filters and wave digital filters, based on LBR two-pair extraction," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 673-686, July 1985.
- [7] G. Péceli, "Structurally passive resonator-based digital filters," to be presented at the 1988 Int. Symp. on Circuits and Systems.
- [8] P. P. Vaidyanathan, "The discrete-time bounded-real lemma in digital filtering," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 918-924, Sept. 1985.
- [9] C. V. K. Prabhakara Rao and P. Dewilde, "On lossless transfer functions and orthogonal realizations," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 677-678, June 1987.
- [10] P. P. Vaidyanathan and V. Liu, "An improved sufficient condition for absence of limit cycles in digital filters," *IEEE Trans. Circuits Syst.*, vol. CAS-34, pp. 319-322, Mar. 1987.
- [11] C. T. Mullis and R. A. Roberts, "Synthesis of minimum roundoff noise fixed point digital filters," *IEEE Trans. Circuits Syst.*, vol. CAS-23, pp. 551-562, Sept. 1976.
- [12] Gong-Tao Yan and S. K. Mitra, "Modified coupled-form digital filter structures," *Proc. IEEE*, vol. 70, pp. 762-763, July 1982.
- [13] T. Saramäki, "On the design of digital filters as a sum of two all-pass filters," *IEEE Trans. Circuits Syst.*, vol. CAS-32, pp. 1191-1193, Nov. 1985.

A Class-C Loop Gain Amplitude Modulator

DAVID J. COMER AND RICHARD HERRON

Abstract—A class-C loop-gain amplitude modulator is reported. This circuit exhibits excellent modulation linearity while requiring a very low level of modulating source power.

INTRODUCTION

The class-A loop-gain amplitude modulator, recently reported in [1], exhibits a high degree of modulation linearity for indexes of modulation approaching unity. This modulator is useful in low-power high-quality applications but cannot compete with class-C stages in high power applications. This paper reports on the extension of the loop-gain modulation concept to the class-C stage. The class-C loop gain circuit not only produces the characteristic high degree of modulation linearity, but also allows the modulating signal to be applied to the base circuit of the transistor modulator. Along with small modulation source current very small modulation voltages are required to achieve large carrier amplitude deviations. This reduces the modulating source power by two or three orders of magnitude over the traditional collector modulation stage.

Manuscript received March 24, 1988. This work was supported by the State of Utah under a Center of Excellence grant. This letter was recommended by Associate Editor A. M. Davis.

The authors are with the Department of Electrical and Computer Engineering, Brigham Young University, Provo, UT 84602.
IEEE Log Number 8825160.

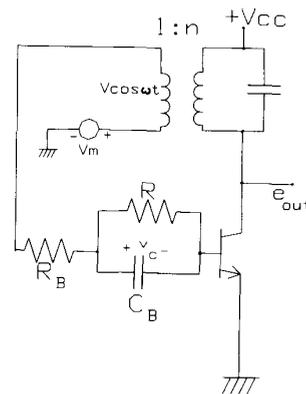


Fig. 1. The class-C loop-gain modulator.

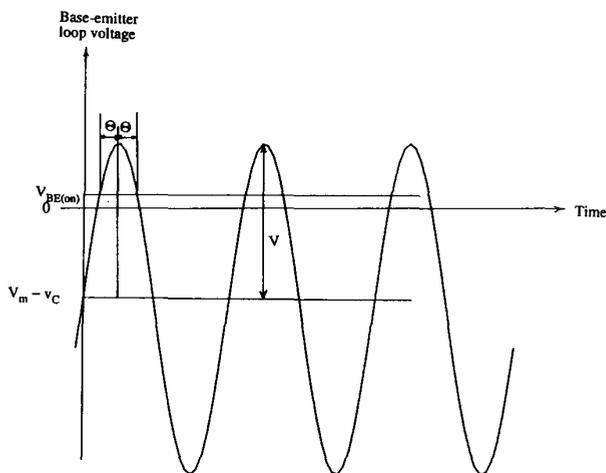


Fig. 2. Definition of θ .

THEORY OF OPERATION

Fig. 1 indicates the configuration of the class-C loop-gain modulator. This circuit operates as a class-C oscillator with the output signal serving as the carrier signal. The tuned collector circuit determines the carrier frequency. The feedback factor from collector-to-base circuit is equal to the reciprocal of the transformer turns ratio or

$$F = \frac{e_f}{e_{out}} = -\frac{1}{n} \tag{1}$$

The forward gain of the circuit is given by [2]

$$A = \frac{-\beta R_p}{R_B} \left[\theta - \frac{\sin 2\theta}{2} \right] \tag{2}$$

where β is the current gain of the transistor from base to collector, θ is one-half of the conduction angle as defined in Fig. 2, and R_p is the resonant tank circuit impedance. The loop gain