Digital Design (VIMIAA01) first homework

Deadline: 3rd November, 2014

Name: …… Personal code: ……

The work can be submitted at any time before the deadline to the lecturer. Please give detailed information about the process of the design work. Final results without appropriate reasoning will be rejected. ***All work should be done in handwriting, but the source code can be printed out! Please use clean A4 papers for your work.***

Design a synchronous 3-bit counter, which presents its possible 8 states on its output in a prescribed order. The order is specified by the digits of your personal code above, extended by a 0 digit at the start.

Task 1: Design a state machine (using a 3-bit register with synchronous reset input) that directly generates the repeating sequence of numbers defined by your personal code. For example, if the personal code is 7312546, then the state transitions should start from 0, then step to 7, to 3, to 1, to 2, to 5, to 4, to 6 and back to 0, according to the requirements. Also, create the Verilog HDL description of the system and verify the design with simulation.

Task 2: Design a second implementation based on a 3-bit binary up-counter. Design binary up-counter using a 3-bit register with synchronous reset input, which generates the numbers from 0 to 7 in natural order (0, 1, 2, 3, 4, 5, 6, 7, 0, 1, 2, …). Complete this counter with an output combinational logic, which remaps the numbers from 0 to 7 in natural order to numbers from 0 to 7 in the order determined by your personal code. For example, if the personal code is 7312546, then combinational logic should remap 0 to 0, 1 to 7, 2 to 3, 3 to 1, 4 to 2, 5 to 5, 6 to 4 and 7 to 6. Also, create the Verilog HDL description of the system and verify the design with simulation.