Digital Design (VIMIAA01) second homework

Deadline: 17th December, 2014

Name: ……

The work can be submitted at any time before the deadline to the lecturer. Please give detailed information about the process of the design work. Final results without appropriate reasoning will be rejected. ***All work should be done in handwriting, but the source code can be printed out. Please use clean A4 papers for your work.***

The task is to implement the hardware and software design of an **8-bit Fibonacci series generator**. The Fibonacci series can be generated using the following recursive formula:

$$F_n = F_{n-1} + F_{n-2}, \text{ where } F_1=0 \text{ and } F_2=1$$

So, the numbers should be

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, ...

If the next element of the series cannot be represented on 8 bits then the generation should be restarted from the beginning (0).

a) Specify the high-level state machine of the Fibonacci series generator and derive the standard controller-datapath implementation from it. Define the detailed hardware realization, create the Verilog HDL description of the system using the known standard functional components and verify the design with simulation. The interface signals should be ***clk***, ***rst*** and ***fib_num[7:0]***. The ***rst*** is a synchronous reset signal which resets the system to its initial state when asserted.

Hint: the Fibonacci series generator can be implemented also as a data dominated design, in this case no controller is required.

b) Assume that you have the MiniRISC processor (it will be presented on the lecture). Create an assembly program which generates the Fibonacci numbers and writes them into the external data memory at address 0x80 (128). You can use the internal register file for temporary variables.

Prepare a document about the project and submit the description of the execution of the task. This document should contain the design decisions, the Verilog source code and the assembly program.