

# Digital Design I

## 2<sup>nd</sup> homework

Deadline: 28<sup>th</sup> November 2011, at the lecture

NAME:..... PERSONAL CODE: .....

The work can be submitted at any time before the deadline to the lecturer.

Design a synchronous 3 bit counter which presents its possible 8 states at the output in a prescribed order. The order is specified by the digits of your PERSONAL CODE above, extended by a 0 digit at the start.

- a. Design a state machine, using a 3 bit register, with synchronous RESET, to directly generate the numbers between 0 to 7 in the order of the digits as defined in your PERSONAL CODE. The state register values directly represent the output values, so if the PERSONAL CODE would be 1237456, then the state transitions would start by 0, then step to 1, to 2, to 3, to 7, to 4, to 6, to 5, and back to 0, according to the requirements.
  
- b. Design a second implementation based on a 3 bit binary counter. Design a binary counter using a 3 bit register, with synchronous RESET, to generate the numbers from 0 – 7 in natural order. Complete this counter with an output combinational logic module, which will remap the numbers from 0 – 7 in natural order to numbers 0 – 7 in the order determined by your PERSONAL CODE. For example if the PERSONAL CODE would be 1237465, than the counter operates as 0,1,2,3,4,5,6,7, 0,1,2,..., but the values at the output will be 0,1,2,3,7,4,6,5,0,1,2..... The combinational logic in this example remaps the values 0 to 0, 1 to 1, 2 to 2, 3 to 3, 4 to 7, 5 to 4, 6 to 6 and 7 to 5.