



BUDAPESTI MŰSZAKI ÉS GAZDASÁGTUDOMÁNYI EGYETEM
VILLAMOSMÉRNÖKI ÉS INFORMATIKAI KAR
MÉRÉSTECHNIKA ÉS INFORMÁCIÓS RENDSZEREK TANSZÉK

Digital Design 2

VIMIA111

Tamás Raikovich

BUTE DMIS

Lecturers

- **Mr. Béla Fehér**
 - Room: I.E.417.
 - E-mail: feher@mit.bme.hu
- **Mr. Tamás Raikovich**
 - Room: I.E.335.
 - E-mail: rtamas@mit.bme.hu
 - Homepage: <http://home.mit.bme.hu/~rtamas>

Requirements

- **Contact hours: 4 hours/week**
 - Lecture: 2 hours/week
 - Practice: 2 hours/week
 - Solving test/exam problems
 - Implementing simple designs on real hardware
- **Mid-term requirements (signature):**
 - 2 homeworks and 1 test
- **Examination period:**
 - Exam

Textbook

- **Frank Vahid: Digital Design
2007, John Wiley & Sons, Inc.**
- **The presentations can be downloaded
from my homepage**

Schedule

- **Recall: previous semester (Digital Design 1)**
 - Chapter 1: Introduction
 - Introduction to the digital systems
 - Binary and hexadecimal number systems
 - ***Source coding (data compression)***
 - *Average code word length, entropy, prefix codes*
 - *Shannon and Huffman algorithms*
 - *Block coding (event space extension)*
 - ***Channel coding (error detection/correction)***
 - *Hamming distance*
 - *Parity code, Hamming code*
 - ***Binary integer number representations***
 - *Unsigned*
 - *Signed: signed magnitude, 1's and 2's complement, offset*
 - ***Position codes: Johnson code, Gray code***

Schedule

- **Recall: previous semester (Digital Design 1)**
 - Chapter 2: Combinational logic design
 - Boolean algebra
 - Logic gates: AND, NAND, OR, NOR, XOR, XNOR, NOT
 - Representation of Boolean functions
 - Truth table, sum of minterm form
 - Functional elements: multiplexers, decoders
 - Chapter 3: Sequential logic design / Controllers
 - Bit storage elements: D flip-flop, register
 - Describing the behavior of sequential circuits: FSMs
 - Implementing sequential circuits: controllers

Schedule

- **Recall: previous semester (Digital Design 1)**
 - A part of Chapter 6: Optimizations
 - Two-level combinational logic size minimization
 - Algebraic method
 - Graphical method: Karnaugh maps
 - Mealey and Moore finite state machines
 - State encoding: one-hot, Gray and output encoding
 - State reduction: implication table, *partition method*
- **I assume that you have knowledge about these**

Schedule

- **In this semester:**
 - Chapter 4: Data path components
 - Chapter 5: Register-Transfer Level (RTL) design
 - Chapter 7: Physical implementation
 - Chapter 9: Hardware description languages
 - Chapter 8: Programmable processors
 - Chapter 6: Optimizations (cont.)
- **The order of the chapters may change**