Measurement 5.: Logic gates

Introduction

The goal of this laboratory is to measure the most important parameters of CMOS logic ICs. For the measurement a digital oscilloscope and a waveform generator are used, thus you should be familiar with these instruments.

Theoretical background

1. Logic levels

Binary values at the inputs and outputs of digital logic elements are represented with a voltage level, the so called logic level. The more positive level is called high level (H) while the more negative level is called low level (L). Due to the parameter deviations and additive noises from the environment logic levels are represented with a voltage range instead of a single voltage value. Voltage ranges at the input and output may differ slightly, though for a given digital logic family voltage ranges specified for the output should be within the range specified for the input to get correct operation. Device data sheets specify the minimum value of the H level and the maximum value of the L level, as Figure 1. shows.

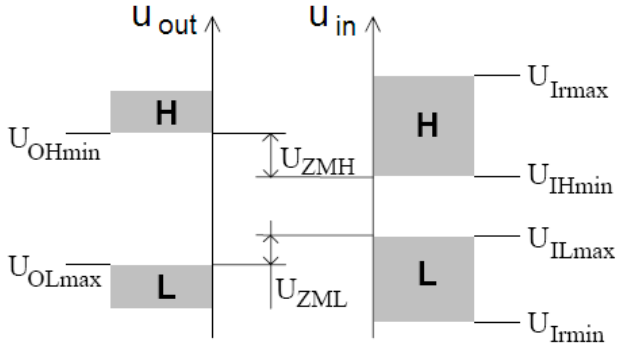

Figure 1. Logic levels

At the input, all voltage levels between U_{Irmin} and U_{ILmax} are treated as logic L and all voltage levels between U_{IHmin} and U_{IRmax} are treated as logic H (going above the specified U_{Irmax} damages the IC!). At the output, for logic L a voltage level below I_{OLmax} is generated; for a logic H, a voltage level above U_{OHmin} is generated.

2. Transfer characteristic and comparison voltage

Voltage transfer characteristic represents how the output voltage changes depending on the input voltage. This characteristic shows how the device behaves when the input voltage differs from the nominal voltage levels.

The point on the characteristic where the input voltage equals to the output voltage is called comparison point – the U_K voltage at this point is referred as comparison voltage. To measure the transfer characteristic, the XY mode of the oscilloscope can be used as shown on Figure 2.

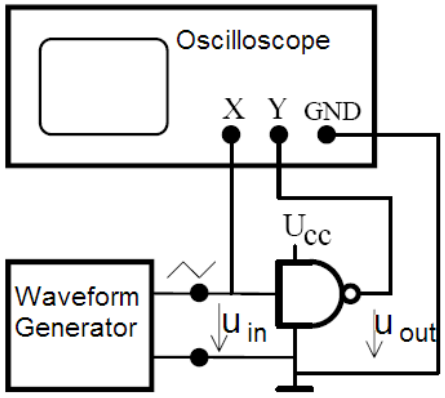

Figure 2. Measuring transfer characteristic

Take care of the followings:

The maximum of the input voltage cannot be higher than the maximum voltage specified for the IC, and the minimum of the input voltage cannot be lower than the minimum voltage specified for the IC. Measure the input signal with the oscilloscope before connecting it the logic device!

Rapidly changing input signals are not appropriate for this measurement, use a triangle wave or a sine wave.

If the ***uout* = f(*uin*) transfer characteristic** is known, the U_K comparison voltage can be easily identified. For non-inverting gates, a line started from the origin with gradient=1 cuts the characteristic at this point.

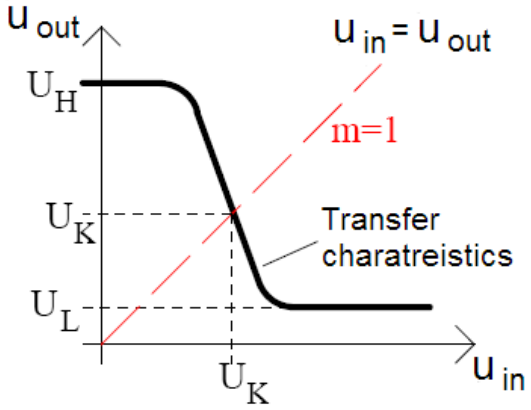

Figure 3. Identifying comparison voltage from the transfer characteristic

3. Noise protection

Due to the environmental noise the logic level may be shifted. This effect can be interpreted with a “clean” original signal with an additive noise signal. Noise protection is defined with the maximum value of the additive noise which does not result in incorrect operation and does not damage the digital device.

The static worst-case noise margin can be computed from the specification with the following equations:

$$U_{ZML} = U_{ILmax} - U_{OLmax}$$

$$U_{ZMH} = U_{OHmin} - U_{IHmin}$$

Typical noise margin can be computed using:

For **L** level: $U_{ZtL} = U_K - U_L$

For **H** level: $U_{ZtH} = U_H - U_K$

Instruments

Oscilloscope	Agilent 54622A
Waveform Generator	Agilent 33220A
PC	NEC TM600
Digital multimeter	Agilent 33401A

Measurement tasks

1. Propagation time of logic gates

Put a 74HC04 CMOS inverter IC into the bottom left ZIF (Zero Insertion Force) socket. As the schematic on the board shows, this IC contains 6 inverters. **NOTE**: Take attention for correct alignment – the IC Pin 1. of the IC should be at the socket end marked with a dot.

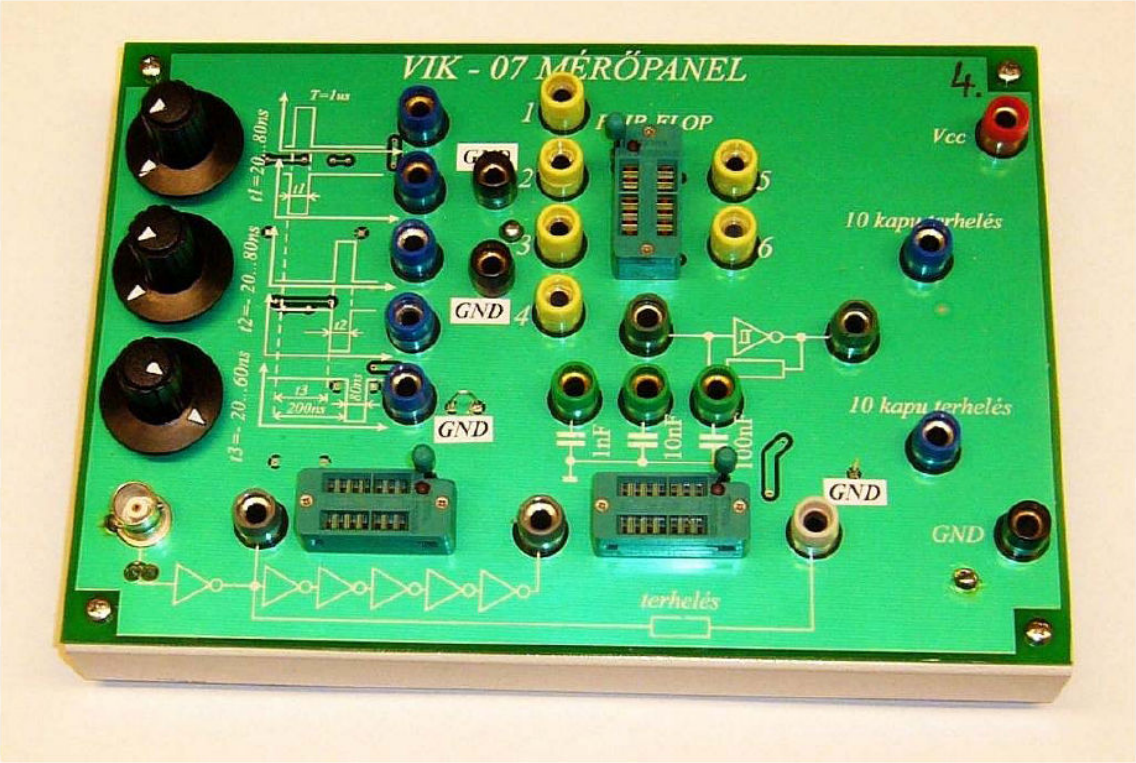

Figure 4. Measurement board

Connect the output of the waveform generator to the input of the inverter (bottom left connector). Use a 50 Ohm coaxial cable and set the output load of the generator to "Hi-Z" (Utility menu).

1.1 Propagation time of a single inverter

Measure the propagation time of the first inverter. Use a 1 MHz square wave with an L level of 0V and H level of 5V (WARNING: using higher voltages damages the IC!).

Connect the oscilloscope to the input and output pins using the scope's measurement cable, as shown on Figure 5.

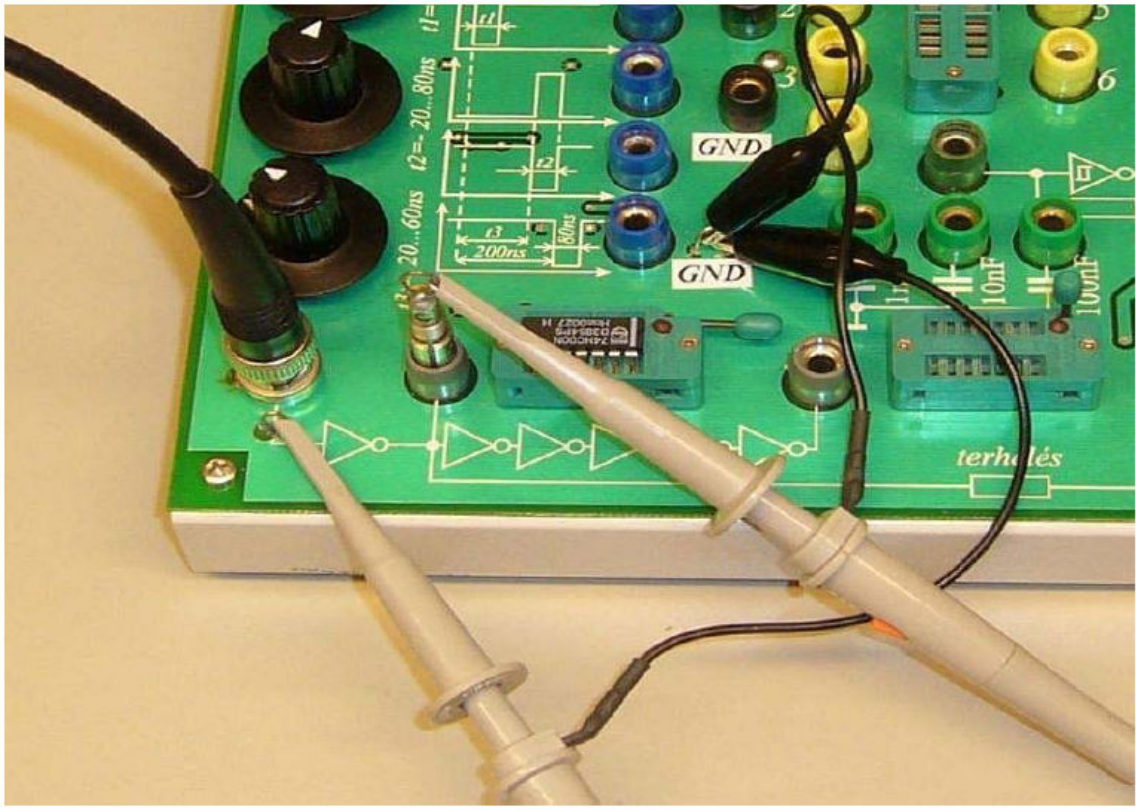

Figure 6. Measuring a single inverter

Use the oscilloscope's cursors to measure the propagation time as shown on Figure 6. For CMOS ICs the comparison voltage UK is defined as the half of the supply voltage.

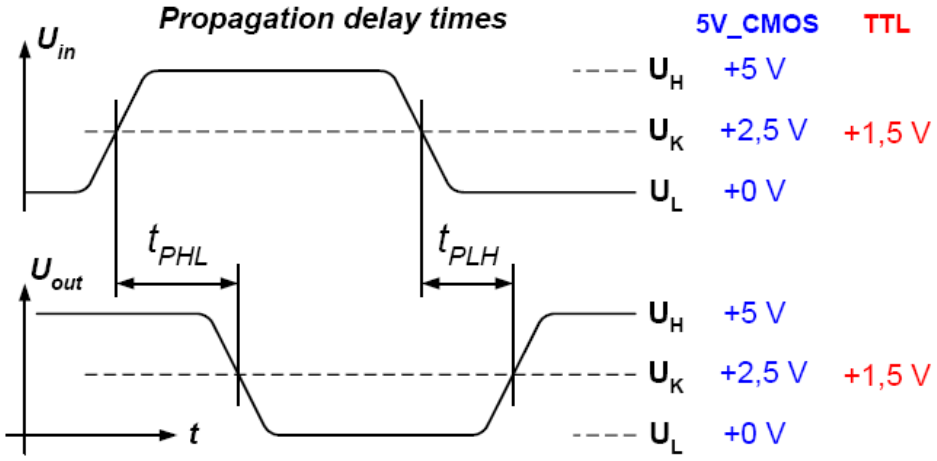

Figure 7. Propagation time

1.2 Propagation time of the inverter chain

Measure the propagation time of the 6 inverters connected into a chain.

Compare the result with the result of a single inverter. The propagation time of six inverters is smaller than six times the propagation time of a single inverter. Why?

2. Output signals of logic gates

2.2 Rise- and fall time

Measure the rise time and fall time at the output of the single inverter using cursors (NOTE: rise- and fall times are defined as the time between the 10% and 90% voltage levels!).

Measure the rise- and fall times using the oscilloscope's built in measurement functions (**`Quick Meas`**urement menu).

3. Comparison voltage

Set the waveform generator to generate a symmetrical triangle wave (50% symmetry). Set L level to 0V and H level to 5V. Connect the inerter input and output the CH0 and CH1 of the oscilloscope.

Set the vertical division of the scope to the same value for both channels and align the 0V (zero levels) of the channel waveforms. The voltage at the intersection point of the two waveforms is the comparison voltage.

Do the same measurement with a low frequency (~10 kHz) triangle wave.

4. Transfer characteristic

4.1 Measure the transfer characteristic

Using the oscilloscope's XY mode measure the transfer characteristic.

4.2 From the transfer characteristic determine:

- Typical L and H levels at the output
- Compariosn voltage

Typical noise margin

5. Setup and propagation time

Put a 74'74 type D flip-flop into the top right socket (again, take attention to correct placement). From the datasheet, determine the function of pins 1 – 6.

Using the board's built in waveform generator create a measurement setup which can be used to measure the setup time of the flip-flop.

Measure:

- Setup time of the flip-flop
- Propagation time of the flip-flop

Help:

For correct operation of a flip-flop, data input should be stable some time before the rising edge of the clock input. This time is referred as the setup time (T_{SU}, Setup Time, Figure 9.).

Propagation time is the time between the rising edge of the clock input and the change at the Q output.

To measure setup time you should be able to generate the waveforms shown on Figure 9.

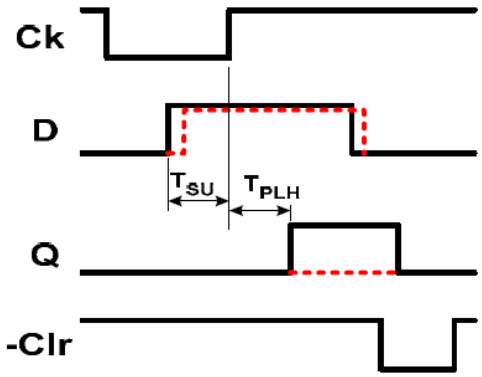

Figure 8. Waveforms for measuring setup time

When the setup time requirement is fulfilled, the FF operates correctly, that is the output changes to logic H. Otherwise the FF may stay in L state or may go into metastable state (the output randomly changes to L or H). Thus, you should be able to move the rising edge at the D input in reference to the rising edge of the clock input.

Test questions

1. What is the transfer characteristic of a logic gate?
2. What is the comparison voltage?
3. How can you determine the comparison voltage from the transfer characteristic?
4. Draw a measurement setup to measure transfer characteristic.
5. Define worst case noise margin.
6. Define typical noise margin.
7. What is the definition of fall time?
9. What is the definition of propagation time for logic gates and for FFs?
10. What is the definition of setup time?
11. What is the definition of hold time?