A Level-Crossing Analog-to-Digital Converter With Triangular Dither

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***Abstract*—In this paper, a level-crossing analog-to-digital converter is described. It can convert audio bandwidth signals with high resolution using few threshold levels and digital interpolation. Samples are generated at nonuniform time intervals and then interpolated to produce uniformly spaced output samples. A periodic triangular dither signal added to the input ensures that low-amplitude or slowly varying signals are sampled and converted accurately. The dither is estimated and removed digitally before interpolation. Simulations show that greater than 10-bit resolution can be achieved with only seven comparators when using a sixth-order polynomial interpolator.**

***Index Terms*—Analog-to-digital (A/D) conversion, dither, interpolation, level-crossing sampling, nonuniform sampling.**

I. Introduction

THERE is an increasing need for CMOS analog-to-digital converters (ADCs) that can be integrated with digital circuits to reduce cost and power dissipation. Nyquist-rate flash ADCs need $2^N - 1$ comparator levels to achieve N bits of resolution. Oversampled ADCs, such as delta--sigma converters, need only a few quantization levels but require a sampling rate much higher than the Nyquist rate.

In general, both Nyquist-rate ADCs and oversampled ADCs sample the input at a fixed rate and quantize the amplitude of the signal. Since sampling occurs at regular time intervals, there is no need to keep track of each sample-time instant. However, in level-crossing ADCs, sampling occurs when the input crosses a comparator threshold [1]. A finite number of threshold levels are used, and only when one of these levels is crossed is a new sample generated. Fig. 1 shows an input signal $y(t)$ and the samples produced by a level-crossing ADC, with comparator thresholds $l_j, j = 1, 2, \ldots, L$. As Fig. 1 shows, the samples may occur at nonuniformly spaced times, since the signal behavior dictates which levels are crossed and when. Therefore, the time instant at which the signal crosses a level must be recorded. If the average sampling rate of the input exceeds twice the input signal bandwidth, the continuous-time input signal could be reconstructed or samples of the input waveform at times other than the sample times t_i could be computed [2]. As the average sampling rate of the input increases, the complexity of an interpolator that computes input samples at times other than the level-crossing times t_i decreases.

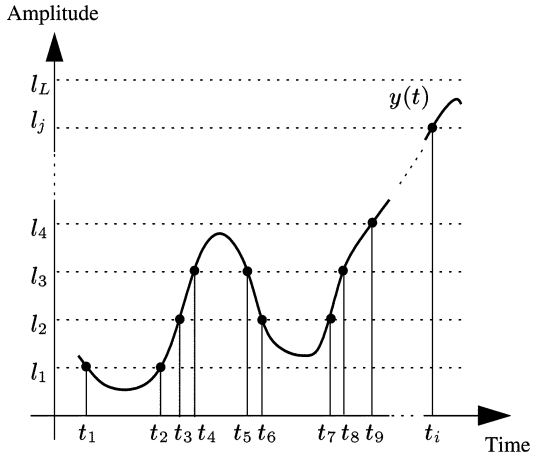

Fig. 1. Nonuniform sampling of input $y(t)$ in a level-crossing ADC. The samples are shown as dots.

This paper describes a mostly digital ADC that is based on a level-crossing architecture [1]. The ADC consists of a simple analog front-end with few comparators, while a digital signal processing (DSP) block is used to generate the digital output at uniformly spaced times. A periodic triangular dither signal is added to the input to increase the input sampling rate for a wide range of input signals. The dither is estimated and removed digitally before interpolation. This architecture is especially suitable for applications where an on-chip digital signal processor is available. In other applications, the overhead in area and power dissipation required for the DSP block is expected to decrease dramatically over time as a result of scaling predicted by Moore's law.

This paper is organized as follows. Section II gives a brief background. Section III introduces the architecture of the level-crossing ADC with triangular dither and describes each block. Simulation results are then presented in Section IV, followed by conclusions in Section V.

II. Background

The idea of using level-crossing sampling for A/D conversion was suggested in 1992 [1]. The ADC architecture is shown in Fig. 2. The input signal $y(t)$ is compared to threshold levels to capture the level-crossing information. The level crossed and the time of crossing are recorded. The time axis is quantized using a fast clock with frequency f_{clk} that is much greater than the input signal bandwidth. Every time the input signal crosses

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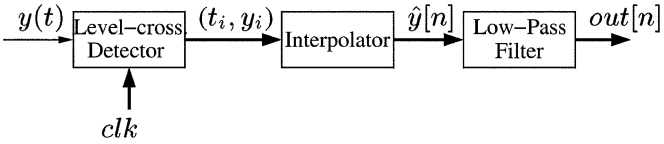

Fig. 2. Level-crossing ADC architecture.

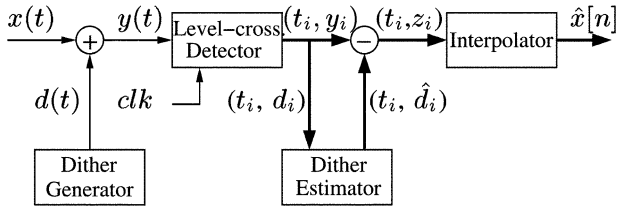

Fig. 3. ADC block diagram.

a level, a new time-amplitude pair (t_i, y_i) is generated and fed to an interpolator. The interpolator converts the time-amplitude pairs to output samples at a specified uniform sampling rate. Finally, the uniform sequence can be filtered by a low-pass filter to reduce out-of-band noise remaining after the interpolation. The output of the final low-pass filter could be decimated to a lower sampling rate. A 14-bit resolution ADC can be built with 64 uniformly spaced threshold levels [3], [4].

In that work, the nonuniformly spaced samples were interpolated with second-order polynomials to produce uniformly spaced output samples at the rate of 128 kHz when using a 4.65-MHz system clock.

Recently, several other nonuniform-sampling-based data converters, called asynchronous data converters, have been reported [5]–[7]. A hybrid delta–sigma level-crossing ADC architecture was described in [7]. The use of cosine dither for zero-crossing sampling and signal reconstruction was suggested in 1984 [8]. The use of cosine dither in a level-crossing ADC for audio signals was proposed in [7]. Simulation results in [7] using 20-kHz cosine dither and 256 threshold levels show that the use of cosine dither can significantly reduce the noise floor in a level-crossing ADC. The dither increases the rate of level crossings and therefore the average sampling rate at the input to the interpolator. Using dither allows the processing of dc inputs.

Generation and removal of the cosine dither were not considered in [7]. Generating a 20-kHz cosine dither signal on an integrated circuit (IC), however, is not easy and requires significant IC area. A digital-to-analog converter (DAC) followed by a low-pass filter could be used. The DAC area would depend on the number of bits needed and the conversion rate. A continuous-time filter with bandwidth near 20 kHz would require a very large IC area for the passive components [9], and the filter bandwidth would vary by $\pm 20\%$ or more due to the effect of process variations on the passive components [10]. Instead, an on-chip 20-kHz oscillator could be used to generate the sinusoidal dither signal. However, the passive components would be very large, and the oscillator output frequency would change from chip to chip due to variations in the passive component values. Variation in the oscillation frequency would introduce variation in the extent to which the cosine dither would be attenuated by a digital filter with a notch at the dither frequency after the interpolator.

In this work, additive triangular dither at 30 kHz is used to reduce the number of threshold levels and ensure that sufficient nonuniformly spaced samples are generated for interpolation for audio bandwidth signals. The dither signal is estimated and subtracted before the interpolator, simplifying the interpolator as explained later. Also, a low-frequency triangular signal is easier to generate on an IC than a comparable sinusoid. Only seven threshold levels, much fewer than in [1], [3], and [7], are used, greatly reducing the size and complexity of the analog blocks. To achieve high resolution, a fast system clock ($f_{\text{clk}} = 500$ MHz) and an interpolator with a sixth-order polynomial are used to convert audio signals.

This architecture relies less on analog techniques and more on digital techniques than in the previous level-crossing ADCs [1], [3], [7]. These characteristics are advantages in modern CMOS processes. Another advantage of this architecture is that it has no stability issues since it does not use feedback. An interesting feature of the level-crossing ADC is that input amplitudes that significantly exceed the outermost threshold levels l_1 and l_L can be handled without severe consequences when using high-order interpolators, since the interpolator can compute sample values outside the range of the threshold levels.

III. ADC Architecture

The block diagram of the ADC architecture is shown in Fig. 3. The ADC consists of a dither generator and level-crossing detector in the analog domain and a dither estimator and signal interpolator in the digital domain. The dither generator produces a triangle wave $d(t)$, which is added to the ADC input $x(t)$. The resulting analog signal $y(t)$ is processed by the L comparators in the level-crossing detector. A high-speed clock is used to quantize and record the instants t_i at which levels are crossed. The level-crossing detector outputs time-amplitude pairs (t_i, y_i). For each output pair, a digital estimate $\hat{d}_i$ of the analog dither signal $d(t)$ at time t_i is produced by the dither estimator and subtracted from the level-crossing value y_i to give $z_i = y_i - \hat{d}_i$. The pairs (t_i, z_i) are interpolated to obtain the uniformly spaced output samples $\hat{x}[n]$, which are digital representations of the input $x(t)$ sampled at a constant sampling period of T.

An alternative approach is to remove the dither after interpolation. Since the interpolator outputs samples that are uniformly spaced in time, linear filtering could be implemented to remove the out-of-band dither. However, when compared to interpolating the input signal that does not include the dither, a much larger number of interpolator coefficients and, consequently, more computation in the digital domain are required to interpolate the input signal plus dither because the triangular dither has frequency content well above the bandwidth of the ADC input $x(t)$. The dither is removed before interpolation to reduce power consumption and area.

The average nonuniform sampling rate at the interpolator input must be at least twice the input signal bandwidth [2] to meet the Nyquist sampling requirement. Without the dither signal, a signal with a small ac amplitude or a dc signal could always fall between level-crossing thresholds and produce no output samples. The dither is added to guarantee an average sampling rate that satisfies the Nyquist criterion for the input $x(t)$, even when the input has a small amplitude or is a dc signal. To ensure frequent level crossings, the frequency of the

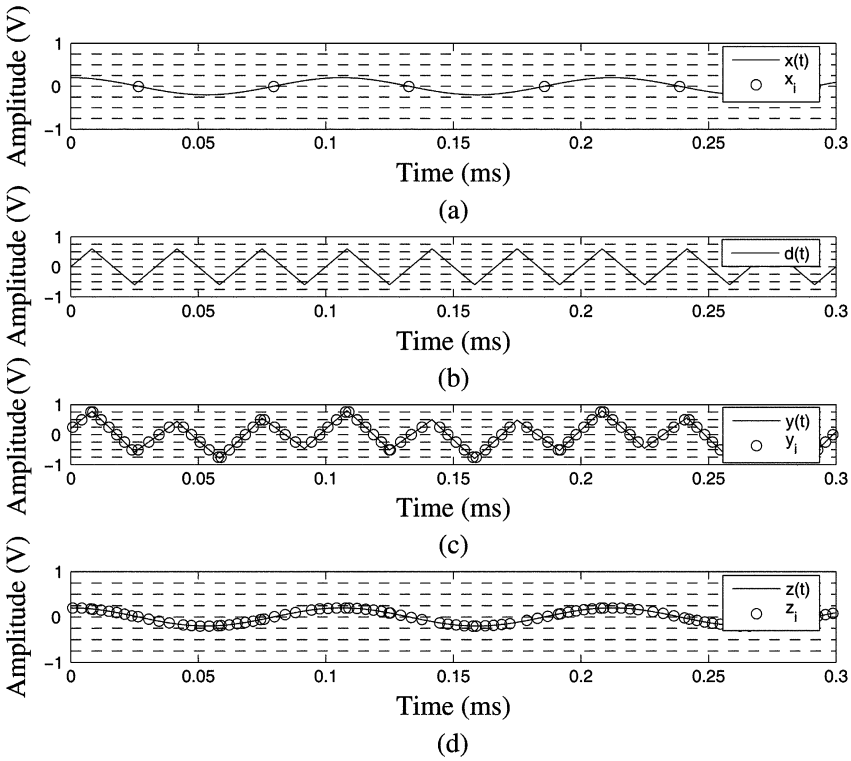

Fig. 4. (a) Samples x_i of the ADC sinusoidal input $x(t)$ with no dither. (b) Triangular dither $d(t)$. (c) The sum $y(t)$ of triangular dither and the input sinusoid and the resulting samples y_i. (d) The signal and samples z_i after the dither has been subtracted from y_i in (c).

triangular dither signal is greater than the bandwidth of the input signal $x(t)$, and the dither signal amplitude is greater than the spacing between level-crossing thresholds. The following sections describe each block in Fig. 3.

A. Dither Generator

The dither generator produces a triangle wave. The fundamental frequency of the triangle wave should be above the bandwidth of the input signal to allow removal of any residual dither signal at the interpolator input by digital low-pass filtering after the interpolator. For good results, a dither amplitude spanning two or more of the threshold levels is desirable, so that even when the ADC input $x(t)$ is small or near dc, time-amplitude pairs are generated by the level-crossing detector once dither is added.

Fig. 4(a) shows a small sinusoidal ADC input $x(t)$ that crosses only one of seven comparator thresholds. Without dither, the resulting samples are marked by the open circles. Since every sample has an amplitude value of zero, the interpolator would generate output samples that are all zero, and the sinusoidal input signal would be lost. If a triangular dither signal is added to the sinusoid in Fig. 4(a) before the level-crossing detector as shown in Fig. 4(b), the resulting input to the level-crossing detector is the waveform shown in Fig. 4(c), which crosses many threshold levels and generates nonzero samples. After the dither has been subtracted, many samples of the input sinusoid remain as shown in Fig. 4(d).

One drawback of the dither signal is increased quantization error, as shown in the next subsection. Also, the use of dither increases the hardware complexity and power consumption of the ADC, and it uses some of the input range of the ADC. However, using dither can dramatically reduce the number of threshold levels needed to achieve high-resolution conversion.

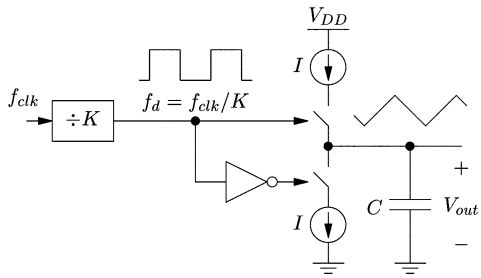

Fig. 5. Simplified, single-ended triangle-wave dither generator.

Fig. 5 shows a simplified schematic of a triangle-wave generator whose output is produced by alternately charging and discharging a capacitor. The charge and discharge times are equal and determined by dividing down the fast clock $f_{\rm clk}$ to produce a square wave with frequency $f_d = f_{\rm clk}/K$, where K is an integer. Therefore, the times at which the slope of the triangle wave changes are known, which simplifies the task of the dither estimator. An example of this type of high-accuracy on-chip triangle-wave generator was demonstrated in [11]. In practice, the triangle-wave generator would be a fully differential circuit. The generated triangle wave would not be ideal, in part due to finite output resistance of the transistor current sources and nonlinear parasitic capacitance in parallel with capacitor C. Nonideal triangular dither is considered in Section III-C.

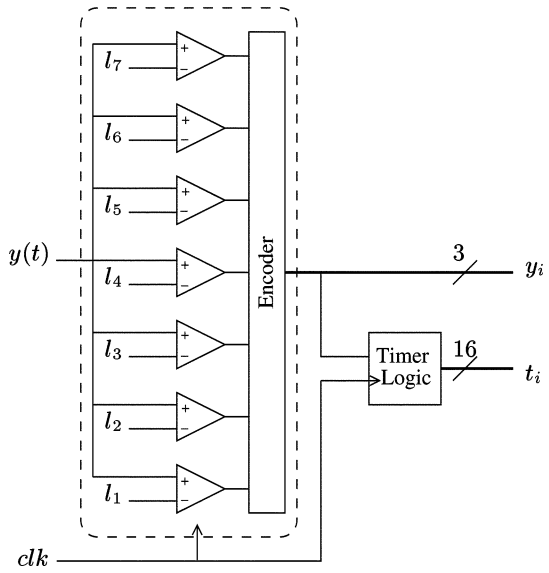

Fig. 6. Level-crossing detector block diagram.

B. Level-Crossing Detector

Fig. 6 shows the level-crossing detector block diagram. The analog input signal $y(t)$ is converted to a digital thermometer-code output using L comparators as in a $\log_2(L+1)$-bit flash ADC. A fast clock signal clk is used to keep track of time. Any change in the thermometer code causes a timer logic block to record the time t_i of the event and the amplitude y_i, which equals the level l_j that is crossed.

Design parameters in this block include the clock period $T_{\text{clk}} = 1/f_{\text{clk}}$ and the number of comparators. The period of the clock, T_{clk}, sets the quantization of the times t_i [1]. An example of the level-crossing-detector input $y(t)$ crossing a threshold level is shown in Fig. 7. When one of the L threshold levels, say l_j, is crossed at level-crossing time t_{LX_i}, the ith amplitude-time pair is recorded in the form (t_i, y_i), where $t_i = k_i T_{\text{clk}}$ and $y_i = y(t_{LX_i}) = l_j$. The actual level crossing may have occurred at any time during the interval $[(k_i-1)T_{\text{clk}}, k_i T_{\text{clk}}]$. Since T_{clk} is nonzero, this introduces a quantization error e_{t_i} in the recorded time t_i

$$e_{t_i} = k_i T_{\text{clk}} - t_{LX_i} \tag{1}$$

which translates to an amplitude error

$$e_{y_i} = y(k_i T_{\text{clk}}) - y(t_{LX_i}). \tag{2}$$

Increasing f_{clk} reduces T_{clk} and reduces these errors.

For sufficiently small T_{clk}, the slope of the input signal to the quantizer, $y'(t)$, is approximately constant near the level crossing and the error in time e_{t_i} can be translated to an error in amplitude using the approximation

$$e_{y_i} \approx y'(t_{LX_i}) e_{t_i}. \tag{3}$$

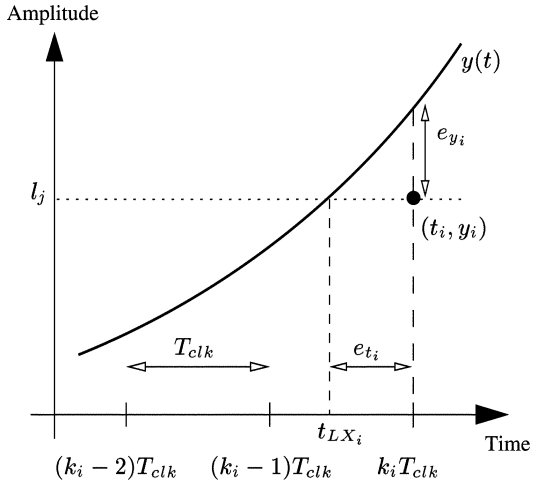

Fig. 7. Error in amplitude e_{y_i} due to quantization in time.

Assuming that $y'(t_{LX_i})$ is statistically independent of $e_{t_i}, y'(t_{LX_i})$ has zero mean and e_{t_i} is uniformly distributed between 0 and T_{clk}, the mean-squared error (MSE) in amplitude due to quantization in time can be calculated

$$E\left[e_y^2\right] = E[y'(t_{LX})^2] E\left[e_t^2\right]. \tag{4}$$

The signal $y(t)$ at the input of the level-crossing detector is

$$y(t) = x(t) + d(t) \tag{5}$$

where $x(t)$ is the signal to be sampled and $d(t)$ is the dither. The dither signal is

$$d(t) = A_d \,\text{triangle}\,(2\pi f_d t) \tag{6}$$

where $\text{triangle}(x)$ is periodic with period 2π and is a straight line connecting -1 to $+1$ during the first half of each period and a straight line connecting $+1$ to -1 during the other half of each period. When $x(t)$ is a sinusoidal signal with frequency f_x, i.e.

$$x(t) = A_x \sin(2\pi f_x t) \tag{7}$$

the derivative of $y(t)$ is

$$y'(t) = x'(t) + d'(t) \tag{8}$$

where

$$x'(t) = (2\pi f_x) A_x \cos(2\pi f_x t) \tag{9}$$

$$d'(t) = \pm 4 A_d f_d. \tag{10}$$

Let $S_x(f)$ denote the power spectrum of $x(t)$. Then, from (8), (9), and (10)

$$E[y'(t_{LX})^2] = \int_{-\infty}^{\infty} (2\pi f)^2 S_x(f) df + (4 f_d A_d)^2 \tag{11}$$

which reduces to

$$E[y'(t_{LX})^2] = 2(\pi f_x A_x)^2 + (4 f_d A_d)^2. \tag{12}$$

If the time quantization has a uniform probability distribution over $[0, T_{\text{clk}}]$, i.e.

$$P(e_t) = \begin{cases} \dfrac{1}{T_{\text{clk}}}, & \text{if } 0 \le t < T_{\text{clk}} \\ 0, & \text{otherwise} \end{cases} \tag{13}$$

the second moment of e_t can be expressed as

$$E\left[e_t^2\right] = \int_0^{T_{\text{clk}}} e_t^2 \frac{1}{T_{\text{clk}}} de_t = \frac{T_{\text{clk}}^2}{3}. \tag{14}$$

From (4), the product of (12) and (14) gives the mean-squared amplitude error

$$E\left[e_y^2\right] = \frac{2}{3}(\pi f_x A_x T_{\text{clk}})^2 + \frac{16}{3}(f_d A_d T_{\text{clk}})^2. \tag{15}$$

When no dither is used, as in [3], $y(t) = x(t)$ and (15) reduces to

$$E\left[e_y^2\right] = \frac{2}{3}(\pi f_x A_x T_{\text{clk}})^2. \tag{16}$$

Thus, when triangular dither is added to the input signal, the MSE on a per-sample basis is increased.

As a side note, if a sinusoidal dither with amplitude A_d and frequency f_d is added to $x(t)$ [7], the second term on the right-hand side of (15) is replaced by $(2/3)(\pi f_d A_d T_{\text{clk}})^2$, and the error becomes slightly larger than with triangular dither. Thus, a benefit of using triangular instead of sinusoidal dither is slightly lower error.

To reduce the MSE, the clock frequency $f_{\text{clk}} = 1/T_{\text{clk}}$ can be increased. From (15), doubling the clock rate reduces the error by 6 dB and increases the ADC's accuracy by 1 bit. However, increasing the clock frequency increases the offset errors in the comparators. Inaccurate comparator thresholds increase the mean-squared amplitude error and reduce the benefits of a fast system clock. For N-bit integral linearity, the level crossings have to be known to N-bit accuracy. Circuit optimization methods and simulations can be used to find a balance between clock speed and comparator accuracy.

To minimize the required analog circuitry, each comparator can add the input and dither signal. For example, a differential comparator with three pairs of inputs (for the ADC input $x(t)$, the dither $d(t)$, and the threshold level l_j) can be realized using three input differential pairs [12] or using multiple input sampling capacitors [13].

The last key parameter in the level-crossing detector block is L, the number of threshold levels. Since the goal is to shift most of the signal processing into the digital domain, L should be kept small. With a low L, however, fewer samples are generated and a higher order polynomial interpolator may be necessary to compute the uniformly spaced sample values. The sampling rate can be increased by increasing the frequency or amplitude of the dither or by adding more comparators. System-level simulations can be used to find a balance between the number of comparators and the interpolation complexity.

C. Dither Estimator

During data conversion, the level-crossing detector produces time-amplitude pairs (t_i, y_i) in the digital domain that represent a sum of the input signal $x(t)$ and dither $d(t)$. To simplify the interpolation, the dither can be removed digitally before the interpolator in one of at least two ways: by subtracting a digital estimate of the analog triangle wave evaluated at the nonuniform time t_i or by nonuniform filtering [14]. Nonuniform filtering is a fairly new topic [15] but may become practical in the near future.

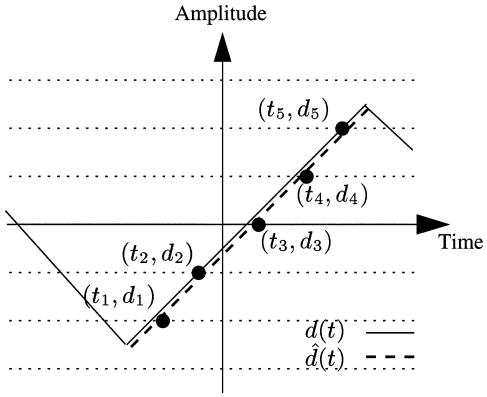

Fig. 8. Ideal dither estimation of a segment with positive slope using $n = 5$ samples.

For this ADC, the dither-free interpolator input (t_i, z_i) is found by digital estimation and subtraction of the dither as shown in Fig. 3. The dither can be measured during a startup period when the ADC input $x(t)$ is set to zero. If only the dither is passed through the level-crossing detector, the time-amplitude pairs (t_i, d_i) output by the level-crossing detector are samples of the dither signal and are processed in the dither estimator to find coefficients that model the triangular dither. When conversion of a nonzero ADC input signal $x(t)$ starts, the sum of the input and dither goes through the level-crossing detector. The previously stored dither coefficients are used to estimate the amplitude of the triangle wave, $\hat{d}_i$, at each time t_i. The resulting $\hat{d}_i$ is subtracted from y_i, greatly reducing the dither at the interpolator input.

1) Ideal Dither: An ideal triangle wave is made up of alternating positively and negatively sloped straight-line segments. After the triangle wave passes through the level-crossing detector, the segments are represented by groups of n nonuniform triangle-wave samples (t_i, d_i). The more levels a segment crosses, the more samples it generates; thus, n depends on the triangle-wave amplitude. For the segment with positive slope in Fig. 8, $n = 5$. As shown in this figure, these nonoverlapping groups of n samples are fit with a straight (dashed) line to estimate the analog dither.

The equation for a positively sloped dither segment is

$$d(t)^+ = \beta_0^+ + \beta_1^+ t \tag{17}$$

where β_0^+ and β_1^+ are the coefficients that need to be calculated. A similar equation is used for a negatively sloped segment

$$d(t)^- = \beta_0^- + \beta_1^- t. \tag{18}$$

Least-squares solutions can be used to estimate the slope and intercept of each segment. Using simple linear regression

$$\hat{\beta}_0^+ = \bar{d} - \hat{\beta}_1^+ \bar{t} \tag{19}$$

$$\hat{\beta}_1^+ = \frac{\sum_{i=1}^{n}(d_i - \bar{d})(t_i - \bar{t})}{\sum_{i=1}^{n}(t_i - \bar{t})^2} \tag{20}$$

where $\bar{t}$ and $\bar{d}$ denote, respectively, the mean values of t_i, and d_i during estimation. The coefficients are estimated for many segments with positive slope (using the known starting time for each segment that is determined by the divider output in Fig. 5), averaged over many segments, and stored in memory for evaluating each $\hat{d}_i$, which is an estimate of the dither at time t_i. Coefficients that describe the segments of the triangle wave with negative slope can be found in a similar manner. Since the estimator finds the best fitting straight-line segment (shown by the dashed line in Fig. 8) given the quantized dither d_i, the estimated triangle wave $\hat{d}(t)$ may be shifted to the right by up to one clock period T_{clk} by time quantization errors. In some applications, correcting for this shift may be beneficial.

2) Nonideal Dither: When the triangular dither is nonideal, the line segments are not perfectly straight, and higher order polynomials are needed to fit each line segment. If fully differential circuits are used to generate the triangular signal, the even harmonics in the nonideal triangle wave should be negligible and only odd harmonics are of concern. If only the third harmonic is significant, the equation for a positively sloped segment of dither can be changed to

$$d(t)^+ = \beta_0^+ + \beta_1^+ t + \beta_3^+ t^3. \tag{21}$$

A similar equation can be used for the negatively sloped segments. Least-squares polynomial approximation can be applied to obtain the coefficients using the same process as in (22) through (24) of the next section.

If other harmonics are significant, the order of the polynomials can be extended, but the complexity of the polynomial interpolator in the dither estimator block would increase. Also, more time would be required to solve for the new coefficients, and more samples would be needed per triangle-wave slope to do the least-squares polynomial approximation. The number of samples per slope can be increased either by increasing the amplitude of the triangle wave so that more levels are crossed or by adding more comparators. Increasing the triangle-wave amplitude increases the mean-squared amplitude error as shown in (15). Adding more comparators increases the analog hardware complexity and power consumption. A compromise can be reached by adding extra comparators and turning them ON only during the startup period when the dither is measured without the input to accurately estimate the nonideal triangle wave.

D. Interpolator

For applications where nonuniformly spaced samples are acceptable, the data conversion process in Fig. 3 could stop after the digital dither is subtracted. However, since most DSP applications require that the ADC output samples be uniformly spaced in time, an interpolator block is usually required to convert from nonuniform to uniform samples. Several different methods can be used to implement the interpolator block: splines [16], wavelets [17], and polynomials [18] to name a few.

For the ADC architecture described in this paper, due to the presence of quantization error in the data, the interpolation is performed with a least-squares polynomial approximation [18]. To fit a given set of nonuniformly spaced time-amplitude pairs, $\{(t_i, z_i) \,|\, i = 1, 2, \ldots, w\}$, with an algebraic polynomial

$$P_m(t) = a_m t^m + a_{m-1} t^{m-1} + \cdots + a_1 t + a_0 \tag{22}$$

of order $m < w - 1$, the constants $a_0, a_1, \ldots, a_m$ must be chosen to minimize the MSE

$$\text{MSE} = \frac{1}{w}\sum_{i=1}^{w}[z_i - P_m(t_i)]^2. \tag{23}$$

The least-squares problem using w nonuniformly spaced samples requires solving the linear system

$$\begin{bmatrix} z_1 \\ z_2 \\ \vdots \\ z_i \\ \vdots \\ z_w \end{bmatrix} = \begin{bmatrix} t_1^m & t_1^{m-1} & \cdots & t_1 & 1 \\ t_2^m & t_2^{m-1} & \cdots & t_2 & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ t_i^m & t_i^{m-1} & \cdots & t_i & 1 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ t_w^m & t_w^{m-1} & \cdots & t_w & 1 \end{bmatrix} \begin{bmatrix} a_m \\ a_{m-1} \\ \vdots \\ a_1 \\ a_0 \end{bmatrix} \tag{24}$$

for the polynomial coefficient vector $\mathbf{a} = [a_m a_{m-1} \ldots a_0]^T$. The solution is unique provided that the sample times t_i are distinct.

For real-time on-chip processing, a sliding window least-squares algorithm [19] can be implemented to obtain the polynomial coefficients without matrix inversions. Each time a new nonuniform sample is acquired, the oldest sample is dropped out of the window (downdating) and the new sample is added (updating). The window size w is determined by the number of nonuniform samples used to compute a set of polynomial coefficients. The approximation is done in a least-squares sense; thus, the number of nonuniform samples in the sliding window should be greater than the polynomial order m.

The rate at which the coefficients are updated is limited by the polynomial order, the window size, the implementation of the sliding window algorithm and the speed of the digital processing block.

The computational complexity of the interpolator can be understood by looking at the number of multiplications required per polynomial, from which one or more output samples are generated. For a simple illustration, assume that QR decomposition [20] is used to evaluate the polynomial coefficients. Obtaining the Vandermonde matrix requires $w(m-1)$ multiplications, generating Q and R each require $w(m+1)^2$ multiplications, and finally, to generate the coefficients, $(m+1)[w + (m+1)/2]$ multiplications are needed. Altogether, the number of multiplications required to obtain one polynomial is

$$M = 2w(m+1)^2 + 2wm + \frac{1}{2}(m^2 + 3m + 2) \tag{25}$$

from which one or more uniformly spaced output samples are obtained. Simulations in the next section were done with a polynomial of order $m = 6$ to fit $w = 9$ nonuniformly spaced samples. Substituting these values in (25) gives 1018 multiplications per polynomial. When the average interpolator output rate is 200 000 samples per second, about 200×10^6 multiplications per second are required (assuming one sample is generated per polynomial). Since some programmable commercial processors

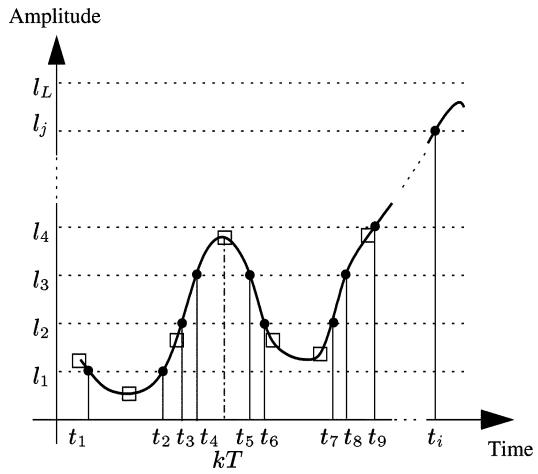

Fig. 9. Nonuniformly spaced samples (circles) from the level-crossing detector and uniformly spaced samples (squares) generated by the interpolator.

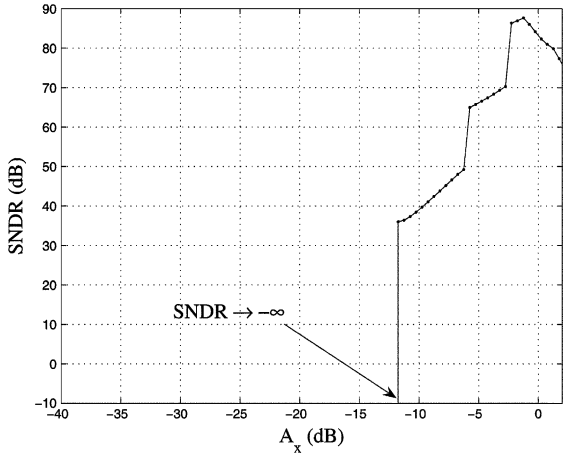

Fig. 10. SNDR versus sinusoidal input amplitude A_x without dither. 0 dB corresponds to a peak sinusoidal amplitude of $A_x = 1.0$ V.

can run at twice this rate, the interpolation is realizable. As IC technology scales in the future, the interpolator order can be increased, which will improve the ADC performance.

Fig. 9 shows an example ADC input waveform, the corresponding nonuniformly sampled output generated by the level-crossing detector (marked with circles), and uniformly spaced samples output by the interpolator (marked with squares). For example, the sample value at time kT can be calculated by the interpolator using the nine samples at times t_1 through t_9.

IV. Simulations

A level-crossing ADC was simulated in MATLAB with the parameters shown in Table I. A sinusoidal input signal was used to find the signal-to-noise-and-distortion ratio (SNDR). Seven threshold levels were used: $0, \pm 0.25$ V, ± 0.5 V, ± 0.75 V. The triangular dither frequency is $f_d = 30$ kHz, and it has an amplitude $A_d = 0.6$ V. The polynomials generated by the interpolator block were evaluated to produce an interpolator output with a sampling rate of 300 kHz. In these simulations, a finite-impulse response (FIR) low-pass filter with 20-kHz bandwidth was used after the interpolator to generate the ADC output (see Fig. 2). The filter attenuates any dither tones that remain after subtraction of the estimate of the triangular dither and interpolation. Also, this filter attenuates excess noise above the signal bandwidth, which is 20 kHz here (for processing audio signals). The output of the FIR filter could be decimated to obtain the output at the Nyquist rate, which is at least twice the bandwidth of the input signal $x(t)$.

The rate at which the ADC samples the input varies, but all simulations gave an average sampling rate of 265 kHz or larger for analog input signals $x(t)$ with various amplitudes and frequencies up to 20 kHz. This sampling rate far exceeds the sampling rate required for a signal with a 20-kHz bandwidth because of the presence of the dither. With no analog input $[x(t) = 0]$, the triangular dither with peak amplitude of 0.6 V crosses ten comparator thresholds (thresholds at $0, \pm 0.25$ V, and ± 0.5 V) each period of the dither. Therefore, the dither alone generates output samples at $10 \times$ 30 kHz $=$300 kHz. When the analog input is added to the dither, the dither ensures a high average sampling rate. The high sampling rate allows accurate interpolation.

TABLE I
ADC Parameters

Parameter	Description	Value
A_x	Input sinusoid amplitude	varies
f_x	Input sinusoid frequency	9.42 kHz
A_d	Peak dither amplitude	0.6 V
f_d	Dither frequency	30 kHz
$f_{clk} = 1/T_{clk}$	System clock frequency	500 MHz
L	Number of levels	7
Δ	Level spacing	0.25 V
m	Polynomial order	6
w	Approximation window size	9

The SNDR was calculated by dividing the power of the desired output signal, which is a scaled version of the ADC input signal, by the power of the undesired noise and distortion at the ADC output

$$\text{SNDR} = 10 \log \left(\frac{\text{signal power}}{\text{noise plus distortion power}} \right) \tag{26}$$

where these powers are measured in $\text{out}[n]$ after the filtering in Fig. 2. This SNDR includes all noise and distortion present in the ADC output $\text{out}[n]$.

Fig. 10 shows the SNDR versus peak input amplitude A_x with a sinusoidal input and without dither. For $A_x < 0.25$ V, only the $l = 0$ level is crossed, and interpolation of the time-amplitude pairs gives a straight line at zero, so the SNDR $\rightarrow -\infty$. The SNDR becomes meaningful only when A_x is large enough so that the ADC input crosses the next level, which corresponds to an input amplitude $A_x = 0.25$ V $= -12$ dB. Every time the input reaches a new threshold level, the SNDR curve jumps.

Fig. 11 shows the same plot for an ideal dither specified in Table I. The SNDR increases at 6 dB/octave over an 84 dB range, peaking at 84.5 dB, the equivalent of about 14 bits. The SNDR drops dramatically at $A_x = 2.6$ dB (or $A_x = 1.35$ V), above which the 0.6-V dither has no effect when the input is near its maximum or minimum value because the outermost

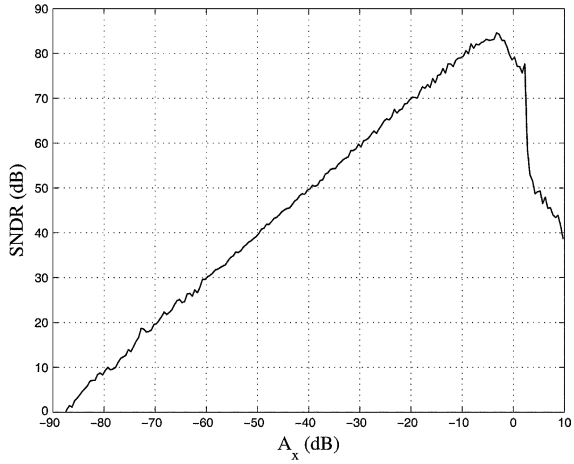

Fig. 11. SNDR versus A_x with ideal dither.

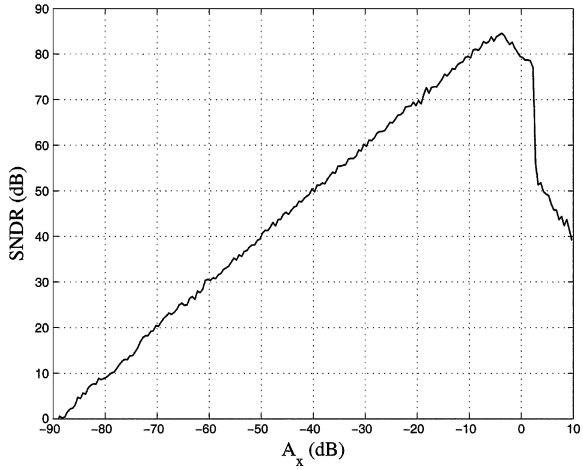

Fig. 12. SNDR versus A_x using nonideal dither that has a third-order nonlinearity as in (27) and a third-order dither estimator.

threshold levels have magnitude 0.75 V. As a result, the average number of samples drops for inputs above this point, reducing the accuracy of the interpolator output. As A_x is increased further, the SNDR decreases gradually from 50 dB downward, unlike in the case of delta--sigma converters, where the SNDR continues to drop sharply. This gradual drop is attributed to the interpolator block being able to estimate samples above full-scale, and this feature may be useful in some applications.

To further increase the ADC's resolution, the parameters in (15) can be adjusted to reduce the quantization error. For example, decreasing the dither amplitude A_d and frequency f_d or increasing $f_{\rm clk}$ can shift the SNDR curve upward. To increase the SNDR near $A_x = 0$ dB, the polynomial order and window size in the interpolator block need to be increased.

To test the performance of the dither estimator for nonideal dither, a dither signal with third-order nonlinearity is used, where the estimator polynomials are of order 3. The actual dither signal used is

$$d_{\rm nonideal}(t) = a_0 + a_1 d(t) + a_3 d^3(t) \tag{27}$$

where $a_0 = 0.1, a_1 = 1.0, a_3 = -0.1$, and $d(t)$ is an ideal triangle wave. Fig. 12 shows the SNDR plot for this case. Since this SNDR plot is almost identical to the result with ideal dither shown in Fig. 11, the dither estimator does a good job at removing the nonideal third-order dither.

Next, a nonideal dither signal with fifth-order nonlinearity is used to test the performance of the dither estimator using a fifth-order polynomial. The nonideal dither signal used here is

$$d_{\rm nonideal}(t) = a_0 + a_1 d(t) + a_3 d^3(t) + a_5 d^5(t) \tag{28}$$

where $a_0 = 0.1, a_1 = 1.0, a_3 = -0.1$, and $a_5 = -0.05$. As mentioned before, to do an overdetermined least-squares polynomial fit, the number of samples generated along each straight-line segment must be greater than the number of coefficients to be estimated. For this example, the dither with fifth-order nonlinearity and a large dc offset requires additional levels to collect sufficient data for a least-squares fit. Two additional comparators with thresholds of ± 0.125 V are added for dither estimation and are turned off during normal ADC operation. Fig. 13 shows

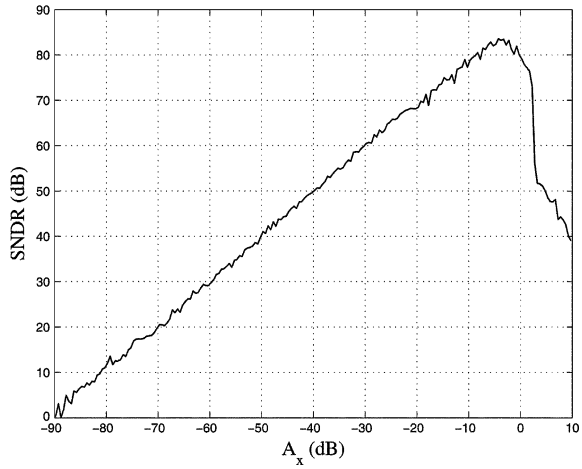

Fig. 13. SNDR versus A_x using nonideal dither with third- and fifth-order nonlinearities as in (28) and a fifth-order dither estimator.

TABLE II
ADC PERFORMANCE

Parameter	Description	Value
f_s	Uniform output sampling frequency	300 kHz
f_{LPF}	Low-pass filter bandwidth	20 kHz
$SNDR_{pk}$	Peak SNDR	83.5-84.5 dB
dyn. range	Dynamic range	84 dB
A_x @ $SNDR_{pk}$	Input amplitude at peak SNDR	−3.25 dB

the SNDR plot when the nonideal dither in (28) is used with a fifth-order estimator for the dither. The plot in Fig. 13 is similar to the one in Fig. 12 except that the peak SNDR here of 83.5 dB is one dB lower and the SNDR plot to the left of the peak dips by 2–3 dB at several places.

In the SNDR plots in Figs. 11–13, the input sinusoid amplitude can reach 2.6 dB (1.35 V) before the SNDR starts to sharply decline. This input amplitude is well above the highest comparator threshold of 0.75 V. Table II summarizes the simulation results for ideal dither and the nonideal dither in (27).

In addition to SNDR plots, a two-tone test was performed with 0.3-V peak amplitude sinusoids at 11.4 kHz and 14.8 kHz,

TABLE III
ADC PARAMETERS FOR THE TWO-TONE TEST

Parameter	Description	Value
A_{x1}	First input sinusoid amplitude	0.3 V
A_{x2}	Second input sinusoid amplitude	0.3 V
f_{x1}	First input sinusoid frequency	11.4 kHz
f_{x2}	Second input sinusoid frequency	14.8 kHz
A_d	Peak dither amplitude	0.6 V
f_d	Dither frequency	30 kHz
f_{clk}	System clock frequency	500 MHz
L	Number of levels	7
Δ	Level spacing	0.25 V
m	Polynomial degree	6
w	Approximation window size	9
$SNDR$	Signal-to-Noise+Distortion Ratio	74.3 dB

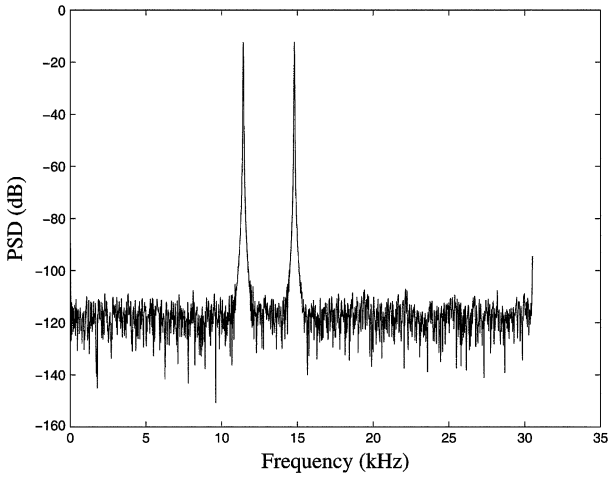

Fig. 14. Power spectral density of ADC interpolator output with two-tone input.

respectively. The ADC interpolator output was sampled at a frequency of 60 kHz. Table III shows the parameters used for this simulation. Note that the 20-kHz FIR low-pass filter was not used here. Ideal triangular dither was used. Fig. 14 shows the ADC output spectrum for this two-tone simulation. The spectrum contains the input tones and a low noise floor, similar to the simulation result in [7]. The small-amplitude tone at 30 kHz is dither that was not removed. A sample-by-sample difference between the (appropriately delayed and sampled) input $x(t)$ and the interpolated output $\hat{x}[n]$ was computed, and the mean-squared value of this difference is 74.3 dB below the total power in the two input sinusoids at 11.4 kHz and 14.8 kHz. The SNDR in this case is 74.3 dB.

Next, nonideal comparator thresholds are considered. Ideally, the spacing between adjacent comparator thresholds is 0.25 V, and all comparator thresholds fall on a straight line. Nonideal comparator thresholds will deviate from a straight line and introduce integral nonlinearity in the ADC. Such nonideality can be modeled by a memoryless nonlinearity $g(y)$ preceding the level-crossing detector as shown in Fig. 15. This nonlinearity distorts the sum of the input $x(t)$ and the dither $d(t)$. A polynomial dither estimator can be used to cancel nonlinear dither terms of the form in (27) and (28) if the dither $d(t)$ is ideal. The distortion that is not canceled may limit the SNDR of the ADC.

For example, consider a nonlinearity given by

$$g(y) = y + c_3 y^3. \tag{29}$$

The sum of the input and the dither, $y(t) = x(t) + d(t)$, passes through $g(y)$. The resulting level-detector output is samples of $\tilde{y}(t)$, where

$$\begin{aligned}\tilde{y}(t) = g(y) &= [x(t) + d(t)] + c_3[x(t) + d(t)]^3 \\ &= x(t) + d(t) + c_3 x^3(t) + c_3 d^3(t) \\ &\quad + 3c_3 x^2(t)d(t) + 3c_3 x(t)d^2(t).\end{aligned} \tag{30}$$

A polynomial dither estimator can generate the dither-only terms $d(t) + c_3 d^3(t)$, and the desired ADC output is $x(t)$. The other terms, $c_3 x^3(t) + 3c_3 x^2(t)d(t) + 3c_3 x(t)d^2(t)$, stem from the nonlinearity and are present in the samples z_i after subtraction of the dither estimate. These remaining terms may degrade the SNDR of the ADC.

Fig. 16 shows the spectrum of the ADC output when a sinusoidal input $x(t) = (0.56\text{ V})\sin[2\pi(4.1\text{ kHz})t]$ is applied to the ADC, and the dither is 0.6 V peak. This input amplitude gives the maximum SNDR of 84.5 dB in Fig. 11. The level-crossing-detector output is processed by the polynomial interpolator and the 20-kHz low-pass filter. Nonideal level-crossing thresholds are used that introduce a nonlinearity as in (29) with $c_3 = 7.98 \times 10^{-4}$. With this c_3, the peak integral nonlinearity is $\text{INL}_{\text{pk}} = 1.9$ LSB (1 LSB $=$ a least-significant bit for a 14 bit ADC), and the $\text{SNDR} = 82.6$ dB. The SNDR is degraded by about 2.0 dB due to the nonlinearity. In the plot, the third harmonic of the input sinusoid, which stems from the $x^3(t)$ term in (30), is visible. A tone near 22 kHz generated by the $x^2(t)d(t)$ term can also be seen in the spectrum.

Under the same conditions with $c_3 = 2.53 \times 10^{-3}$, $\text{INL}_{\text{pk}} = 6.0$ LSB, and the $\text{SNDR} = 75.5$ dB. With $c_3 = 1.01 \times 10^{-2}$, $\text{INL}_{pk} = 22.4$ LSB, and the $\text{SNDR} = 63.8$ dB. Therefore, errors in the level-crossing thresholds introduce integral nonlinearity that may limit performance, as would be the case with any ADC. The amount of ADC nonlinearity that can be tolerated is determined by the application.

To investigate the filtering implemented by the polynomial interpolator, simulations of Fig. 3 were run without added dither [i.e., $d(t) = 0$], without the dither estimator, and without the 20-kHz FIR low-pass filter. The input $x(t)$ is a sinusoid of amplitude 0.56 V, which gives the peak SNDR in Fig. 11. Fig. 17 shows the SNDR measured at the interpolator output. This plot shows the effective low-pass filtering provided by the time-varying interpolator. The SNDR at low frequencies here is less than the peak SNDR in Fig. 11 due to the absence of the dither.

In practice, imperfections in the analog circuits could limit the performance of the level-crossing ADC to below that predicted by the MATLAB simulations. The accuracy of the final ADC output is limited by the accuracy of the data fed into the interpolator. The threshold levels could deviate from their ideal values and introduce nonlinearity as described earlier. Also, imperfect comparator operation could introduce errors. The dither signal

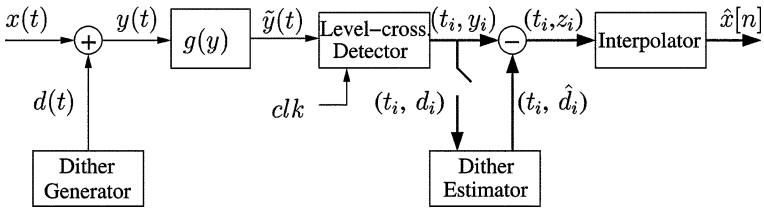

Fig. 15. ADC block diagram including $g(y)$ that models nonlinearity in the level-crossing detector.

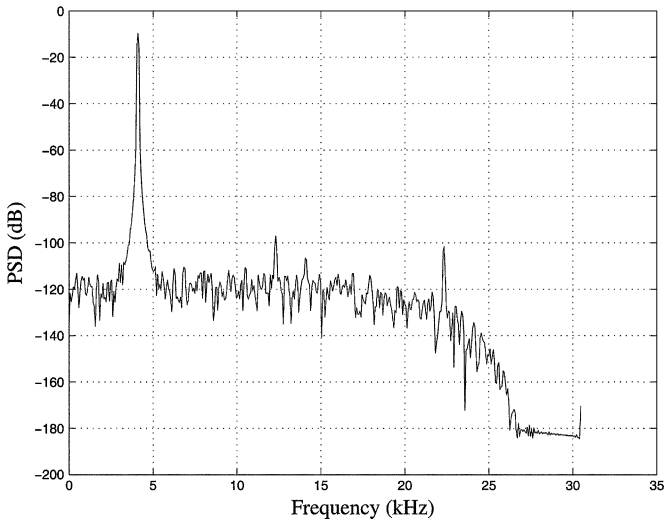

Fig. 16. Power spectral density of the ADC output with third-order nonlinearity.

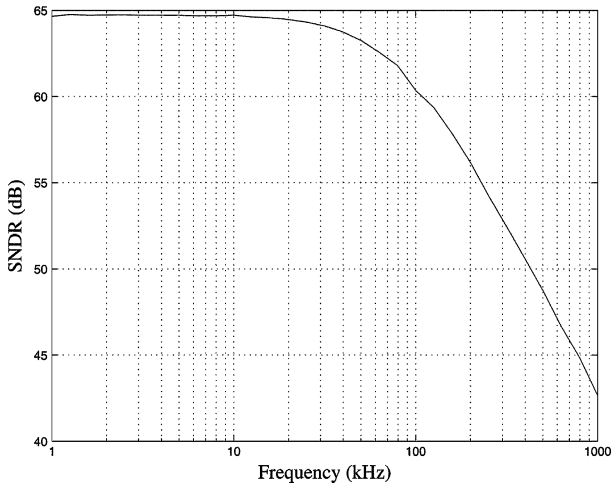

Fig. 17. SNDR versus input frequency for the polynomial interpolator. The input is a sinusoid without dither.

might deviate from an ideal triangle wave, which was considered earlier.

Calibration is a possible way to improve the SNDR above the limit set by the imperfect analog circuits. The goal of calibration would be to learn (in digital form) the actual threshold levels with sufficient accuracy, and then these digitized threshold levels would be used by the interpolator.

In practice, only three comparators are needed at any given time because just after the input crosses level l_j, the next level crossed can only be l_{j-1}, l_j, or l_{j+1}. (If either outermost level l_1 or l_L was just crossed, then only two comparators are needed to record the next level crossing.) Any unused comparators could be turned off to save power or could be taken off-line for calibration. Calibration is a potential future research topic for level-crossing ADCs.

To achieve the peak SNDR from ideal MATLAB simulations, the noise introduced by analog circuits must be much less than the ideal noise floor from simulations. If noise from the analog circuits exceeds the noise floor from ideal simulations, the analog circuit noise would limit the peak SNDR, as is the case in some delta–sigma converters.

V. Conclusion

A level-crossing ADC is proposed with an architecture that uses few analog circuits and complex DSP that can be efficiently built in modern CMOS IC technologies. A high-frequency system clock provides accurate nonuniformly spaced time-amplitude pairs at seven level crossings, while sixth-order polynomial interpolation in the digital domain generates uniformly spaced output samples. Triangular dither is added before the level-crossing detector to meet (and exceed) the Nyquist sampling criterion. The triangular dither is estimated and subtracted before the interpolator, thereby improving the interpolation.

The proposed ADC is similar to delta–sigma converters in that the required number of comparators is small; the DSP circuits are somewhat complex, and the output is oversampled. In contrast, a key difference from delta–sigma converters is that the proposed ADC does not use feedback, thereby avoiding stability problems, and does not require a highly linear integrator. As a result of using additive triangular dither and a high-order interpolator, the proposed ADC can process dc inputs as well as inputs that sometimes exceed the outermost threshold levels.

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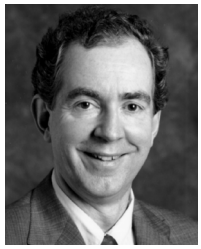

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