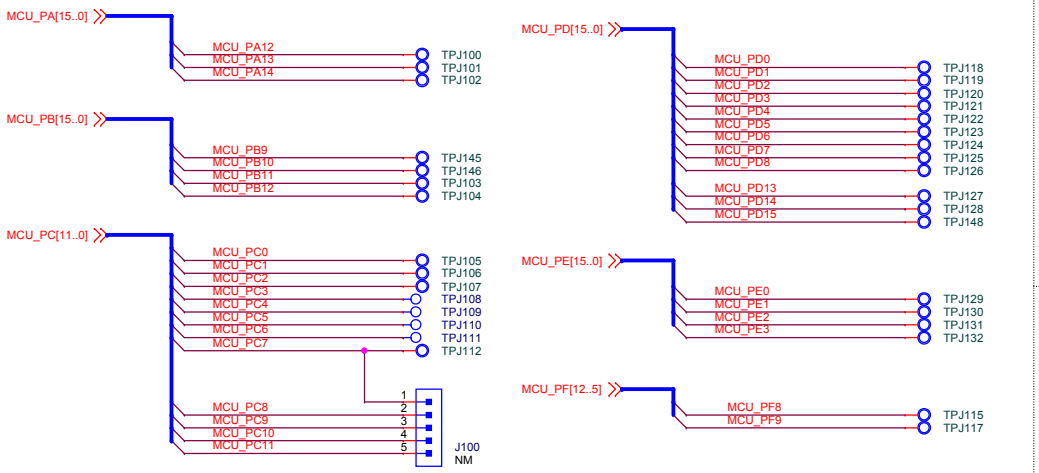
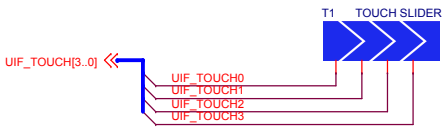
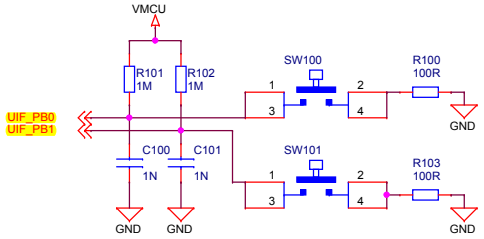
Breakout Connections



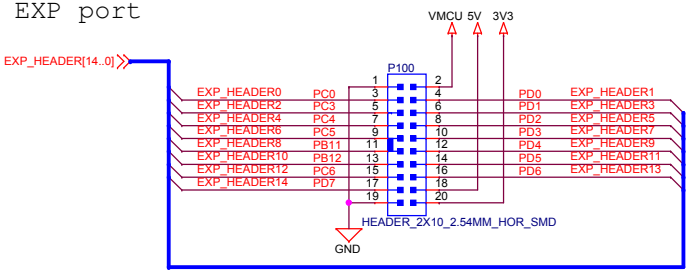
Touch Slider



User pushbuttons



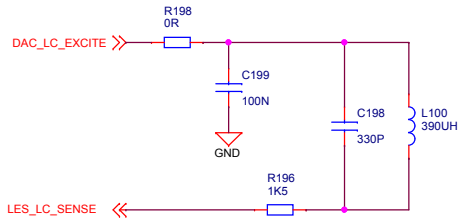
EXP port



EXP Communication

SPI	MOSI-PD0 MISO-PD1 CLK-PD2 CS-PD3
I2C1	SDA-PC4 SCL-PC5
UART	TX-PD0 RX-PD1
LEUART	TX-PD4 RX-PD5

LESENSE LC-Sensor



Power

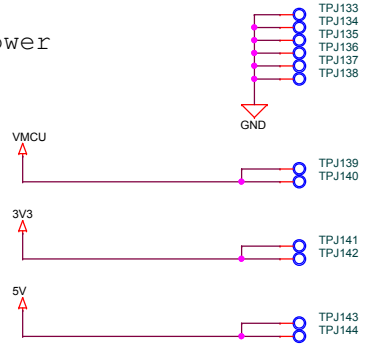
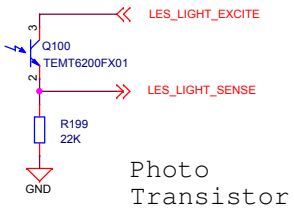
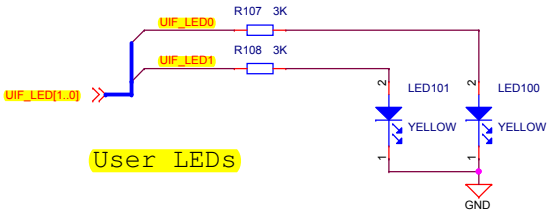


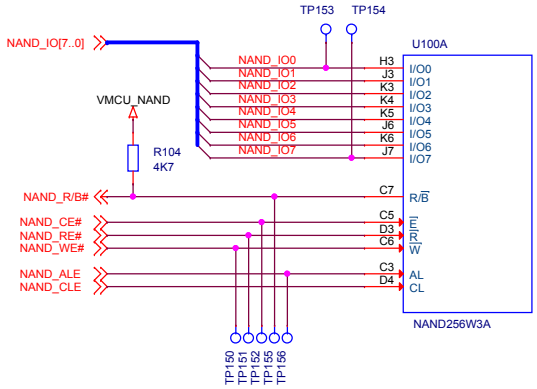
Photo Transistor

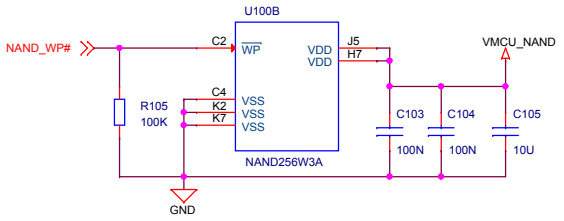


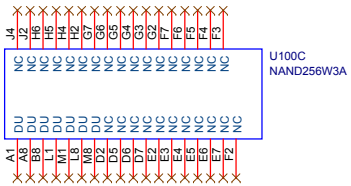
User LEDs



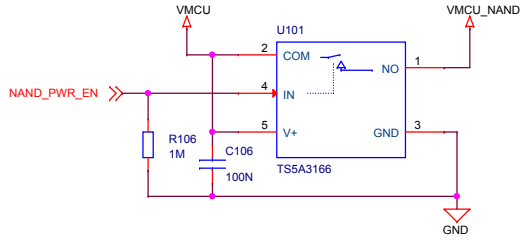
32MB NAND Flash







NAND Power



STK

SILICON LABS

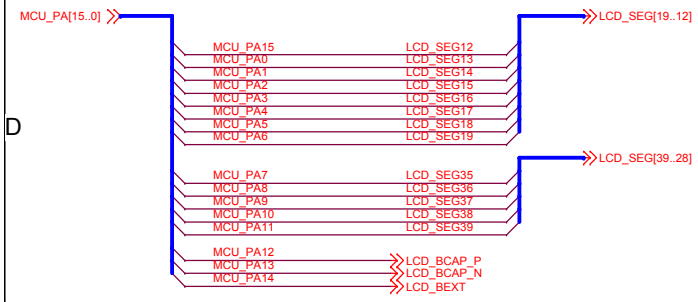
Designed: DDB	Approved: JNO
Size A3	BOM Doc No:
Design Created Date: Wednesday, December 03, 2008	

Schematic Title: **EFM32 Giant Gecko Starter Kit**

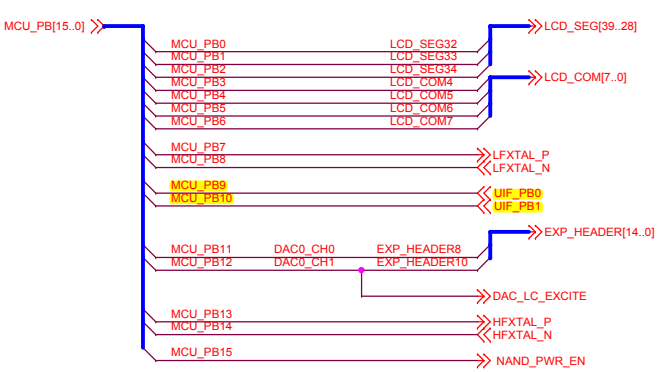
Page Title: **User Interfaces**

Document number: BRD2200A	Revision: A03
Sheet Created Date: Saturday, March 21, 2009	Sheet Modified Date: Tuesday, April 18, 2017
	Sheet 2 of 10

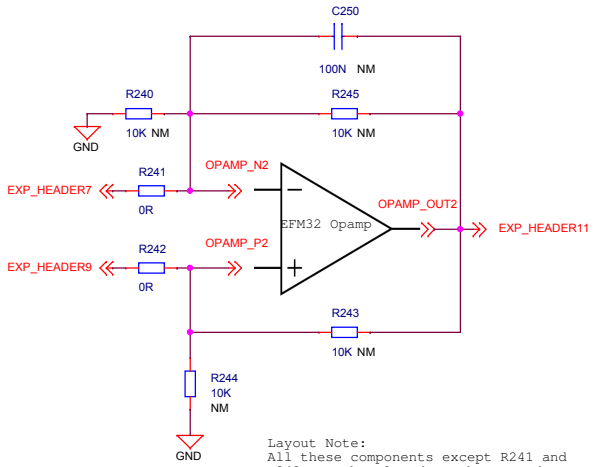
PA Connections



PB Connections

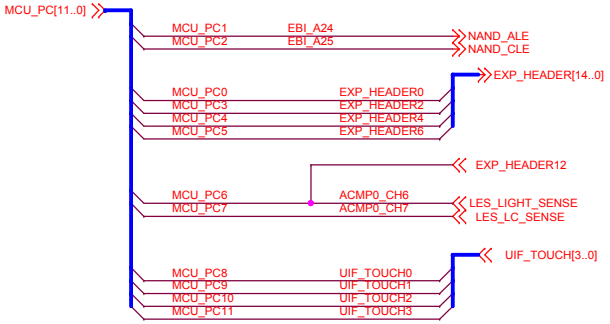


OPAMP Connection Footprint

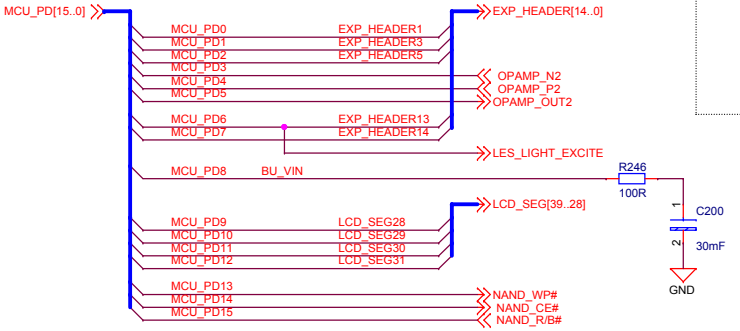


Layout Note:
All these components except R241 and R242 must be placed on the secondary side, and are not to be mounted in production.

PC Connections

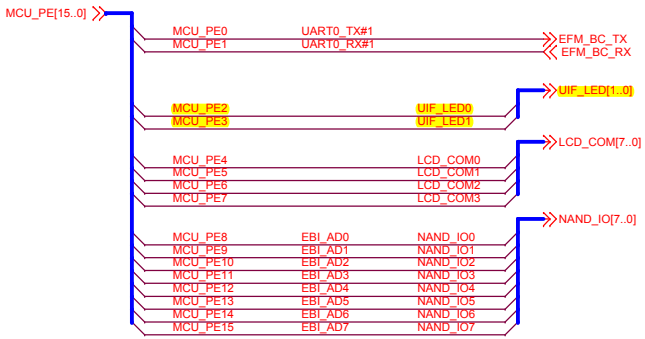


PD Connections

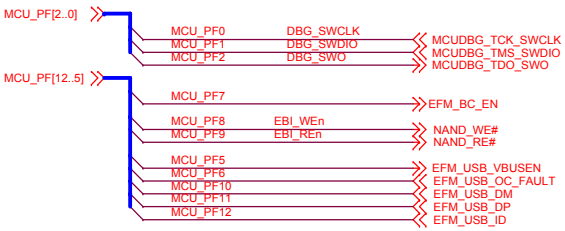


Capacitor for Backup Power Domain

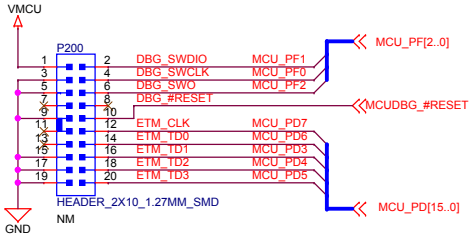
PE Connections



PF Connections



19-pin JTAG/SWD and Trace connector footprint (reverse side)



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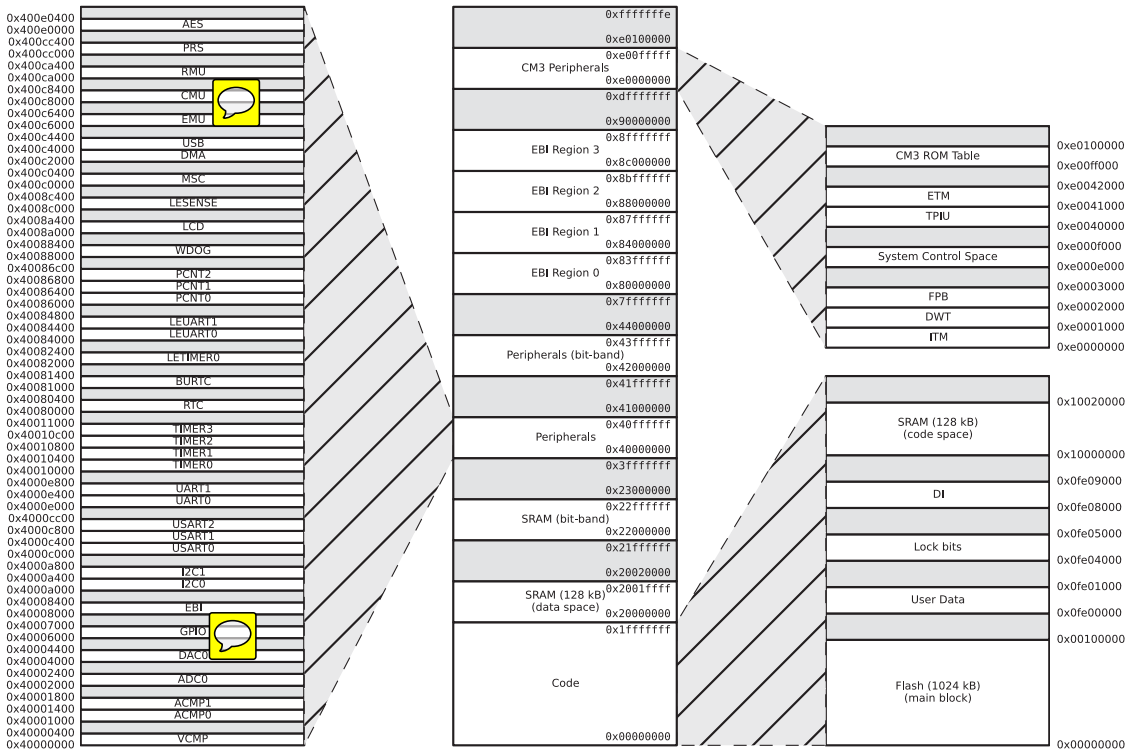
Design Created Date: Wednesday, December 03, 2008	

Schematic Title
EFM32 Giant Gecko Starter Kit

Page Title
Signal Assignments

Document number: BRD2200A	Revision: A03
Sheet Created Date: Friday, January 15, 2010	Sheet Modified Date: Tuesday, April 18, 2017
	Sheet 3 of 10

Figure 5.2. System Address Space



The embedded SRAM is located at address 0x20000000 in the memory map of the EFM32GG. When running code located in SRAM starting at this address, the Cortex-M3 uses the System bus to fetch instructions. This results in reduced performance as the Cortex-M3 accesses stack, other data in SRAM and peripherals using the System bus. To be able to run code from SRAM efficiently, the SRAM is also mapped in the code space at address 0x10000000. When running code from this space, the Cortex-M3 fetches instructions through the I/D-Code bus interface, leaving the System bus for data access. The SRAM mapped into the code space can however only be accessed by the CPU, i.e. not the DMA.

5.2.1 Bit-banding

The SRAM bit-band alias and peripheral bit-band alias regions are located at 0x22000000 and 0x42000000 respectively. Read and write operations to these regions are converted into masked single-bit reads and atomic single-bit writes to the embedded SRAM and peripherals of the EFM32GG.

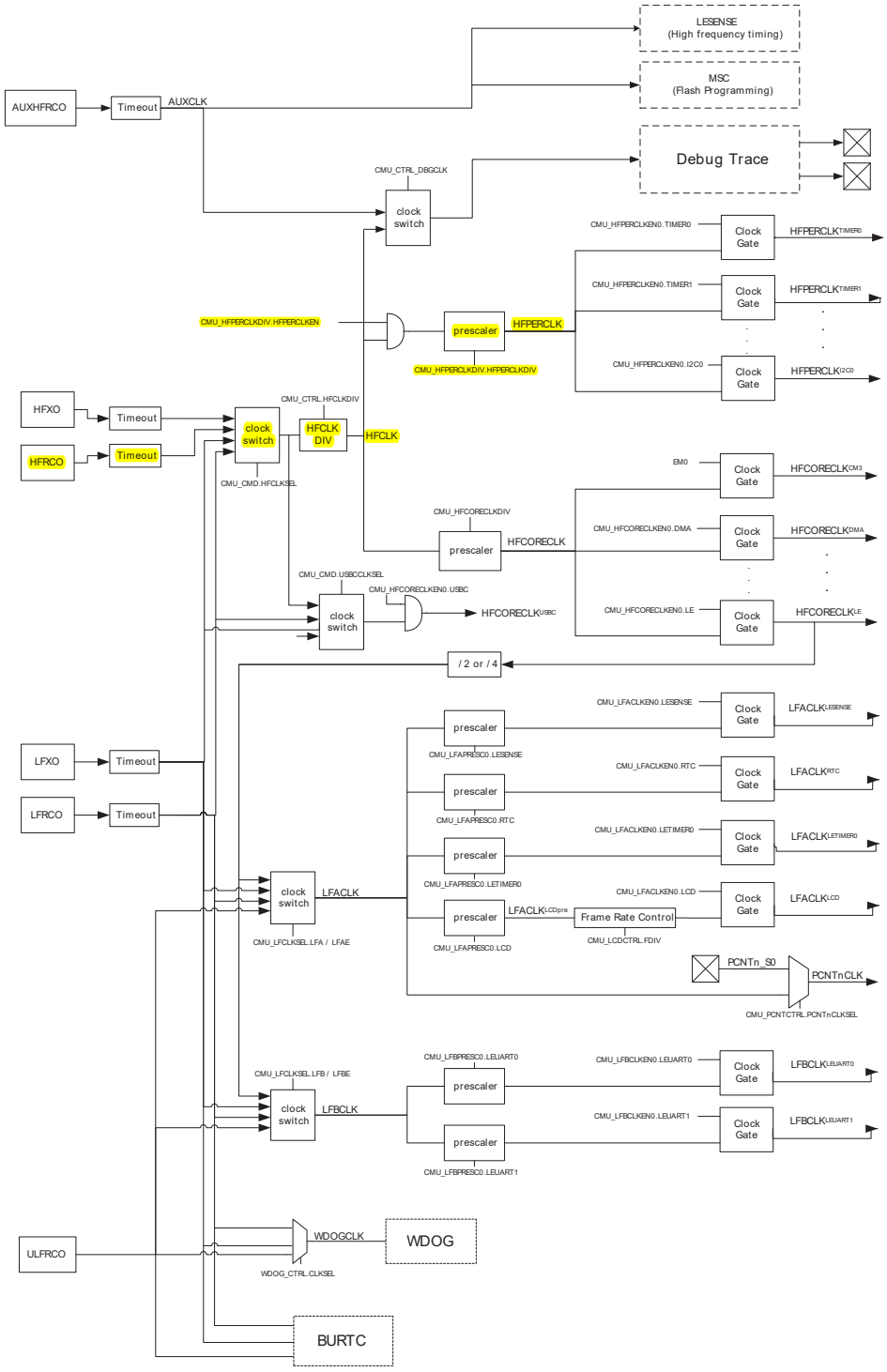
The standard approach to modify a single register or SRAM bit in the aliased regions, requires software to read the value of the byte, half-word or word containing the bit, modify the bit, and then write the byte, half-word or word back to the register or SRAM address. Using bit-banding, this read-modify-write can be done in a single atomic operation. As read-writeback, bit-masking and bit-shift operations are not necessary in software, code size is reduced and execution speed improved.

The bit-band regions allows addressing each individual bit in the SRAM and peripheral areas of the memory map. To set or clear a bit in the embedded SRAM, write a 1 or a 0 to the following address:

Memory SRAM Area Set/Clear Bit

$$bit\_address = 0x22000000 + (address - 0x20000000) \times 32 + bit \times 4, \quad (5.1)$$

Figure 11.1. CMU Overview



11.3.1 System Clocks

11.3.1.1 HFCLK - High Frequency Clock

HFCLK is the selected High Frequency Clock. This clock is used by the CMU and drives the two prescalers that generate HFCORECLK and HFPERCLK. The HFCLK can be driven by a high-frequency oscillator (HFRCO or HFXO) or one of the low-frequency oscillators (LFRCO or LFXO). By default the HFRCO is selected. In most applications, one of the high frequency oscillators will be the preferred

11.4 Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	CMU_CTRL	RW	CMU Control Register
0x004	CMU_HFCORECLKDIV	RW	High Frequency Core Clock Division Register
0x008	CMU_HFPERCLKDIV	RW	High Frequency Peripheral Clock Division Register
0x00C	CMU_HFRCOCTRL	RW	HFRCO Control Register
0x010	CMU_LFRCOCTRL	RW	LFRCO Control Register
0x014	CMU_AUXHFRCOCTRL	RW	AUXHFRCO Control Register
0x018	CMU_CALCTRL	RW	Calibration Control Register
0x01C	CMU_CALCNT	RWH	Calibration Counter Register
0x020	CMU_OSCENCMD	W1	Oscillator Enable/Disable Command Register
0x024	CMU_CMD	W1	Command Register
0x028	CMU_LFCLKSEL	RW	Low Frequency Clock Select Register
0x02C	CMU_STATUS	R	Status Register
0x030	CMU_IF	R	Interrupt Flag Register
0x034	CMU_IFS	W1	Interrupt Flag Set Register
0x038	CMU_IFC	W1	Interrupt Flag Clear Register
0x03C	CMU_IEN	RW	Interrupt Enable Register
0x040	CMU_HFCORECLKEN0	RW	High Frequency Core Clock Enable Register 0
0x044	CMU_HFPERCLKEN0	RW	High Frequency Peripheral Clock Enable Register 0
0x050	CMU_SYNCBUSY	R	Synchronization Busy Register
0x054	CMU_FREEZE	RW	Freeze Register
0x058	CMU_LFACLKEN0	RW	Low Frequency A Clock Enable Register 0 (Async Reg)
0x060	CMU_LFBCLKEN0	RW	Low Frequency B Clock Enable Register 0 (Async Reg)
0x068	CMU_LFAPRESC0	RW	Low Frequency A Prescaler Register 0 (Async Reg)
0x070	CMU_LFBPRESC0	RW	Low Frequency B Prescaler Register 0 (Async Reg)
0x078	CMU_PCNTCTRL	RW	PCNT Control Register
0x07C	CMU_LCDCTRL	RW	LCD Control Register
0x080	CMU_ROUTE	RW	I/O Routing Register
0x084	CMU_LOCK	RW	Configuration Lock Register

11.5.3 CMU_HFPERCLKDIV - High Frequency Peripheral Clock Division Register

Offset	Bit Position																															
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																								1						0x0		
Access																								RW						RW		
Name																								HFPERCLKEN						HFPERCLKDIV		

Bit	Name	Reset	Access	Description
31:9	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
8	HFPERCLKEN	1	RW	**HFPERCLK Enable**
	Set to enable the HFPERCLK.			
7:4	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
3:0	HFPERCLKDIV	0x0	RW	**HFPERCLK Divider**
	Specifies the clock divider for the HFPERCLK.			

Value	Mode	Description
0	HFCLK	HFPERCLK = HFCLK.
1	HFCLK2	HFPERCLK = HFCLK/2.
2	HFCLK4	HFPERCLK = HFCLK/4.
3	HFCLK8	HFPERCLK = HFCLK/8.
4	HFCLK16	HFPERCLK = HFCLK/16.
5	HFCLK32	HFPERCLK = HFCLK/32.
6	HFCLK64	HFPERCLK = HFCLK/64.
7	HFCLK128	HFPERCLK = HFCLK/128.
8	HFCLK256	HFPERCLK = HFCLK/256.
9	HFCLK512	HFPERCLK = HFCLK/512.

11.5.4 CMU_HFRCOCTRL - HFRCO Control Register

Offset	Bit Position																															
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x00					0x3			0x80							
Access																	RW					RW			RW							
Name																	SUDELAY					BAND			TUNING							

Bit	Name	Reset	Access	Description
31:17	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
16:12	SUDELAY	0x00	RW	**HFRCO Start-up Delay**
	Always write this field to 0.			
11	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		

Bit	Name	Reset	Access	Description
31:6	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
5	EBI	0	RW	**External Bus Interface Clock Enable**
	Set to enable the clock for EBI.			
4	LE	0	RW	**Low Energy Peripheral Interface Clock Enable**
	Set to enable the clock for LE. Interface used for bus access to Low Energy peripherals.			
3	USB	0	RW	**Universal Serial Bus Interface Clock Enable**
	Set to enable the clock for USB.			
2	USBC	0	RW	**Universal Serial Bus Interface Core Clock Enable**
	Set to enable the clock for USBC.			
1	AES	0	RW	**Advanced Encryption Standard Accelerator Clock Enable**
	Set to enable the clock for AES.			
0	DMA	0	RW	**Direct Memory Access Controller Clock Enable**
	Set to enable the clock for DMA.			

11.5.18 CMU_HFPERCLKEN0 - High Frequency Peripheral Clock Enable Register 0

Offset	Bit Position																													
0x044	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset															0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access															RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Name															DAC0	ADC0	PRS	VCMP	GPIO	I2C1	I2C0	ACMP1	ACMP0	TIMER3	TIMER2	TIMER1	TIMER0	UART1	UART0	USART2	USART1	USART0

Bit	Name	Reset	Access	Description
31:18	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
17	DAC0	0	RW	**Digital to Analog Converter 0 Clock Enable**
	Set to enable the clock for DAC0.			
16	ADC0	0	RW	**Analog to Digital Converter 0 Clock Enable**
	Set to enable the clock for ADC0.			
15	PRS	0	RW	**Peripheral Reflex System Clock Enable**
	Set to enable the clock for PRS.			
14	VCMP	0	RW	**Voltage Comparator Clock Enable**
	Set to enable the clock for VCMP.			
13	GPIO	0	RW	**General purpose Input/Output Clock Enable**
	Set to enable the clock for GPIO.			
12	I2C1	0	RW	**I2C 1 Clock Enable**
	Set to enable the clock for I2C1.			
11	I2C0	0	RW	**I2C 0 Clock Enable**
	Set to enable the clock for I2C0.			
10	ACMP1	0	RW	**Analog Comparator 1 Clock Enable**
	Set to enable the clock for ACMP1.			
9	ACMP0	0	RW	**Analog Comparator 0 Clock Enable**
	Set to enable the clock for ACMP0.			

32.4 Register Map

The offset register address is relative to the registers base address.

Offset	Name	Type	Description
0x000	GPIO_PA_CTRL	RW	Port Control Register
0x004	GPIO_PA_MODEL	RW	Port Pin Mode Low Register
0x008	GPIO_PA_MODEH	RW	Port Pin Mode High Register
0x00C	GPIO_PA_DOUT	RW	Port Data Out Register
0x010	GPIO_PA_DOUTSET	W1	Port Data Out Set Register
0x014	GPIO_PA_DOUTCLR	W1	Port Data Out Clear Register
0x018	GPIO_PA_DOUTTGL	W1	Port Data Out Toggle Register
0x01C	GPIO_PA_DIN	R	Port Data In Register
0x020	GPIO_PA_PINLOCKN	RW	Port Unlocked Pins Register
0x024	GPIO_PB_CTRL	RW	Port Control Register
0x028	GPIO_PB_MODEL	RW	Port Pin Mode Low Register
0x02C	GPIO_PB_MODEH	RW	Port Pin Mode High Register
0x030	GPIO_PB_DOUT	RW	Port Data Out Register
0x034	GPIO_PB_DOUTSET	W1	Port Data Out Set Register
0x038	GPIO_PB_DOUTCLR	W1	Port Data Out Clear Register
0x03C	GPIO_PB_DOUTTGL	W1	Port Data Out Toggle Register
0x040	GPIO_PB_DIN	R	Port Data In Register
0x044	GPIO_PB_PINLOCKN	RW	Port Unlocked Pins Register
0x048	GPIO_PC_CTRL	RW	Port Control Register
0x04C	GPIO_PC_MODEL	RW	Port Pin Mode Low Register
0x050	GPIO_PC_MODEH	RW	Port Pin Mode High Register
0x054	GPIO_PC_DOUT	RW	Port Data Out Register
0x058	GPIO_PC_DOUTSET	W1	Port Data Out Set Register
0x05C	GPIO_PC_DOUTCLR	W1	Port Data Out Clear Register
0x060	GPIO_PC_DOUTTGL	W1	Port Data Out Toggle Register
0x064	GPIO_PC_DIN	R	Port Data In Register
0x068	GPIO_PC_PINLOCKN	RW	Port Unlocked Pins Register
0x06C	GPIO_PD_CTRL	RW	Port Control Register
0x070	GPIO_PD_MODEL	RW	Port Pin Mode Low Register
0x074	GPIO_PD_MODEH	RW	Port Pin Mode High Register
0x078	GPIO_PD_DOUT	RW	Port Data Out Register
0x07C	GPIO_PD_DOUTSET	W1	Port Data Out Set Register
0x080	GPIO_PD_DOUTCLR	W1	Port Data Out Clear Register
0x084	GPIO_PD_DOUTTGL	W1	Port Data Out Toggle Register
0x088	GPIO_PD_DIN	R	Port Data In Register
0x08C	GPIO_PD_PINLOCKN	RW	Port Unlocked Pins Register
0x090	GPIO_PE_CTRL	RW	Port Control Register
0x094	GPIO_PE_MODEL	RW	Port Pin Mode Low Register
0x098	GPIO_PE_MODEH	RW	Port Pin Mode High Register
0x09C	GPIO_PE_DOUT	RW	Port Data Out Register

Offset	Name	Type	Description
0x0A0	GPIO_PE_DOUTSET	W1	Port Data Out Set Register
0x0A4	GPIO_PE_DOUTCLR	W1	Port Data Out Clear Register
0x0A8	GPIO_PE_DOUTTGL	W1	Port Data Out Toggle Register
0x0AC	GPIO_PE_DIN	R	Port Data In Register
0x0B0	GPIO_PE_PINLOCKN	RW	Port Unlocked Pins Register
0x0B4	GPIO_PF_CTRL	RW	Port Control Register
0x0B8	GPIO_PF_MODEL	RW	Port Pin Mode Low Register
0x0BC	GPIO_PF_MODEH	RW	Port Pin Mode High Register
0x0C0	GPIO_PF_DOUT	RW	Port Data Out Register
0x0C4	GPIO_PF_DOUTSET	W1	Port Data Out Set Register
0x0C8	GPIO_PF_DOUTCLR	W1	Port Data Out Clear Register
0x0CC	GPIO_PF_DOUTTGL	W1	Port Data Out Toggle Register
0x0D0	GPIO_PF_DIN	R	Port Data In Register
0x0D4	GPIO_PF_PINLOCKN	RW	Port Unlocked Pins Register
0x100	GPIO_EXTIPSELL	RW	External Interrupt Port Select Low Register
0x104	GPIO_EXTIPSELH	RW	External Interrupt Port Select High Register
0x108	GPIO_EXTIRISE	RW	External Interrupt Rising Edge Trigger Register
0x10C	GPIO_EXTIFALL	RW	External Interrupt Falling Edge Trigger Register
0x110	GPIO_IEN	RW	Interrupt Enable Register
0x114	GPIO_IF	R	Interrupt Flag Register
0x118	GPIO_IFS	W1	Interrupt Flag Set Register
0x11C	GPIO_IFC	W1	Interrupt Flag Clear Register
0x120	GPIO_ROUTE	RW	I/O Routing Register
0x124	GPIO_INSENSE	RW	Input Sense Register
0x128	GPIO_LOCK	RW	Configuration Lock Register
0x12C	GPIO_CTRL	RW	GPIO Control Register
0x130	GPIO_CMD	W1	GPIO Command Register
0x134	GPIO_EM4WUEN	RW	EM4 Wake-up Enable Register
0x138	GPIO_EM4WUPOL	RW	EM4 Wake-up Polarity Register
0x13C	GPIO_EM4WUCAUSE	R	EM4 Wake-up Cause Register

32.5 Register Description

32.5.1 GPIO_Px_CTRL - Port Control Register

Offset	Bit Position																													
0x000	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																															0x0	
Access																															RW	
Name																															DRIVEMODE	

Bit	Name	Reset	Access	Description
31:2	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
1:0	DRIVEMODE	0x0	RW	**Drive Mode Select**

Select drive mode for all pins on port configured with alternate drive strength.

Value	Mode	Description
0	STANDARD	6 mA drive current
1	LOWEST	0.1 mA drive current
2	HIGH	20 mA drive current
3	LOW	1 mA drive current

32.5.2 GPIO_Px_MODEL - Port Pin Mode Low Register

Offset	Bit Position																													
0x004	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE7				MODE6				MODE5				MODE4				MODE3				MODE2				MODE1				MODE0			

Bit	Name	Reset	Access	Description
31:28	MODE7	0x0	RW	**Pin 7 Mode**
	Configure mode for pin 7. Enumeration is equal to MODE0.			
27:24	MODE6	0x0	RW	**Pin 6 Mode**
	Configure mode for pin 6. Enumeration is equal to MODE0.			
23:20	MODE5	0x0	RW	**Pin 5 Mode**
	Configure mode for pin 5. Enumeration is equal to MODE0.			
19:16	MODE4	0x0	RW	**Pin 4 Mode**
	Configure mode for pin 4. Enumeration is equal to MODE0.			
15:12	MODE3	0x0	RW	**Pin 3 Mode**
	Configure mode for pin 3. Enumeration is equal to MODE0.			
11:8	MODE2	0x0	RW	**Pin 2 Mode**
	Configure mode for pin 2. Enumeration is equal to MODE0.			
7:4	MODE1	0x0	RW	**Pin 1 Mode**
	Configure mode for pin 1. Enumeration is equal to MODE0.			
3:0	MODE0	0x0	RW	**Pin 0 Mode**

Configure mode for pin 0.

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set
2	INPUTPULL	Input enabled. DOUT determines pull direction
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction
4	PUSHPULL	Push-pull output
5	PUSHPULLDRIVE	Push-pull output with drive-strength set by DRIVEMODE
6	WIREDOR	Wired-or output
7	WIREDORPULLDOWN	Wired-or output with pull-down
8	WIREDAND	Open-drain output
9	WIREDANDFILTER	Open-drain output with filter
10	WIREDANDPULLUP	Open-drain output with pullup
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup
12	WIREDANDDRIVE	Open-drain output with drive-strength set by DRIVEMODE

Bit	Name	Reset	Access	Description

Value	Mode	Description
13	WIREDANDDRIVEFILTER	Open-drain output with filter and drive-strength set by DRIVEMODE
14	WIREDANDDRIVEPULLUP	Open-drain output with pullup and drive-strength set by DRIVEMODE
15	WIREDANDDRIVEPULLUPFILTER	Open-drain output with filter, pullup and drive-strength set by DRIVEMODE

32.5.3 GPIO_Px_MODEH - Port Pin Mode High Register

Offset	Bit Position																													
0x008	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0x0				0x0				0x0				0x0				0x0				0x0				0x0				0x0			
Access	RW				RW				RW				RW				RW				RW				RW				RW			
Name	MODE15				MODE14				MODE13				MODE12				MODE11				MODE10				MODE9				MODE8			

Bit	Name	Reset	Access	Description
31:28	MODE15	0x0	RW	**Pin 15 Mode**
	Configure mode for pin 15. Enumeration is equal to MODE8.			
27:24	MODE14	0x0	RW	**Pin 14 Mode**
	Configure mode for pin 14. Enumeration is equal to MODE8.			
23:20	MODE13	0x0	RW	**Pin 13 Mode**
	Configure mode for pin 13. Enumeration is equal to MODE8.			
19:16	MODE12	0x0	RW	**Pin 12 Mode**
	Configure mode for pin 12. Enumeration is equal to MODE8.			
15:12	MODE11	0x0	RW	**Pin 11 Mode**
	Configure mode for pin 11. Enumeration is equal to MODE8.			
11:8	MODE10	0x0	RW	**Pin 10 Mode**
	Configure mode for pin 10. Enumeration is equal to MODE8.			
7:4	MODE9	0x0	RW	**Pin 9 Mode**
	Configure mode for pin 9. Enumeration is equal to MODE8.			
3:0	MODE8	0x0	RW	**Pin 8 Mode**
	Configure mode for pin 8.			

Value	Mode	Description
0	DISABLED	Input disabled. Pullup if DOUT is set.
1	INPUT	Input enabled. Filter if DOUT is set
2	INPUTPULL	Input enabled. DOUT determines pull direction
3	INPUTPULLFILTER	Input enabled with filter. DOUT determines pull direction
4	PUSHPULL	Push-pull output
5	PUSHPULLDRIVE	Push-pull output with drive-strength set by DRIVEMODE
6	WIREDOR	Wired-or output
7	WIREDORPULLDOWN	Wired-or output with pull-down
8	WIREDAND	Open-drain output
9	WIREDANDFILTER	Open-drain output with filter
10	WIREDANDPULLUP	Open-drain output with pullup
11	WIREDANDPULLUPFILTER	Open-drain output with filter and pullup
12	WIREDANDDRIVE	Open-drain output with drive-strength set by DRIVEMODE
13	WIREDANDDRIVEFILTER	Open-drain output with filter and drive-strength set by DRIVEMODE
14	WIREDANDDRIVEPULLUP	Open-drain output with pullup and drive-strength set by DRIVEMODE
15	WIREDANDDRIVEPULLUPFILTER	Open-drain output with filter, pullup and drive-strength set by DRIVEMODE

32.5.4 GPIO_Px_DOUT - Port Data Out Register

Offset	Bit Position																													
0x00C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0000															
Access																	RW															
Name																	DOUT															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
15:0	DOUT	0x0000	RW	**Data Out**
	Data output on port.			

32.5.5 GPIO_Px_DOUTSET - Port Data Out Set Register

Offset	Bit Position																													
0x010	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0000															
Access																	W1															
Name																	DOUTSET															

Bit	Name	Reset	Access	Description
31:16	*Reserved*	*To ensure compatibility with future devices, always write bits to 0. More information in Section 2.1 (p. 3)*		
15:0	DOUTSET	0x0000	W1	**Data Out Set**
	Write bits to 1 to set corresponding bits in GPIO_Px_DOUT. Bits written to 0 will have no effect.			

32.5.6 GPIO_Px_DOUTCLR - Port Data Out Clear Register

Offset	Bit Position																													
0x014	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																	0x0000															
Access																	W1															
Name																	DOUTCLR															