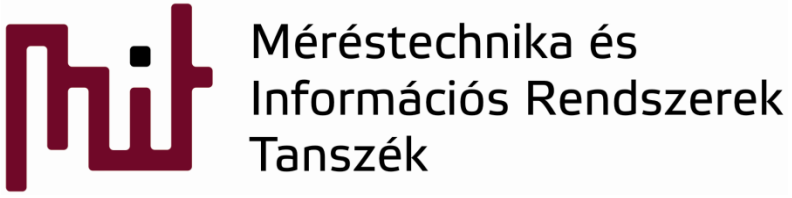
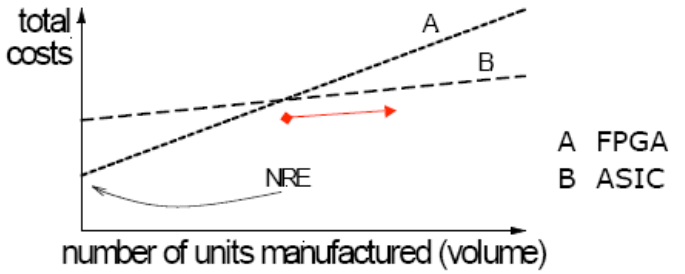
Embedded and Ambient Systems
2022.12.06.

FPGA (Field Programable Gate Array)



FPGA: evolution

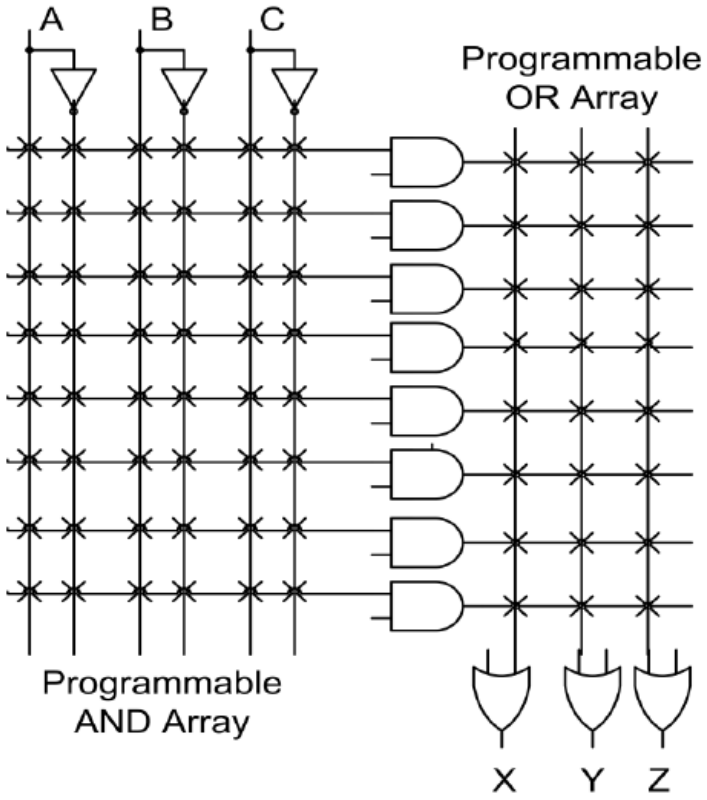
- Dynamically configurable devices
- When applying FPGA a system is built up based on basic digital circuit elements
- Motivation:
  - Solve problems based on digital HW:
    - Rapid operation
    - Slow development
      - Production time is long
        - » In the past (mainly): printed circuit board + discrete logic gates
        - » Today: ASIC (Application Specific Integrated Circuits)
        - » NRE: Non-recurring engineering
      - Testing and re-design take a long time: slow iterations
  - Time to market is important, therefore the development process needs to be accelerated



- A device is needed that is suitable for the implementation of low level functions but the production and development time is shorter

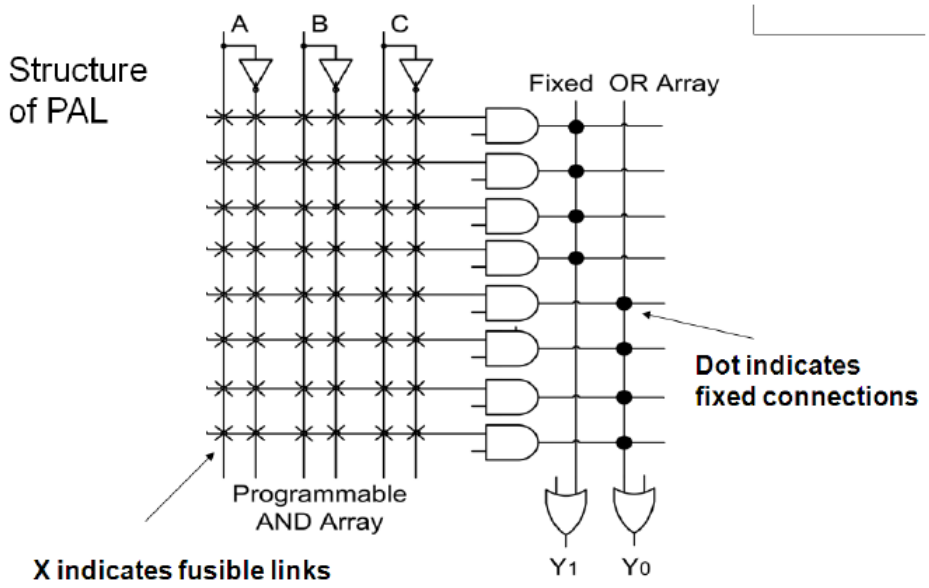
FPGA: evolution

- PLA: Programmable Logic Array
  - In 1970s
  - Programmable AND and OR gates
  - Implementation of logical functions in canonical form
  - Advancement: special circuit for the implementation of complex logic functions
  - Drawback: PLSs can be configured during production process and cannot be reconfigured later



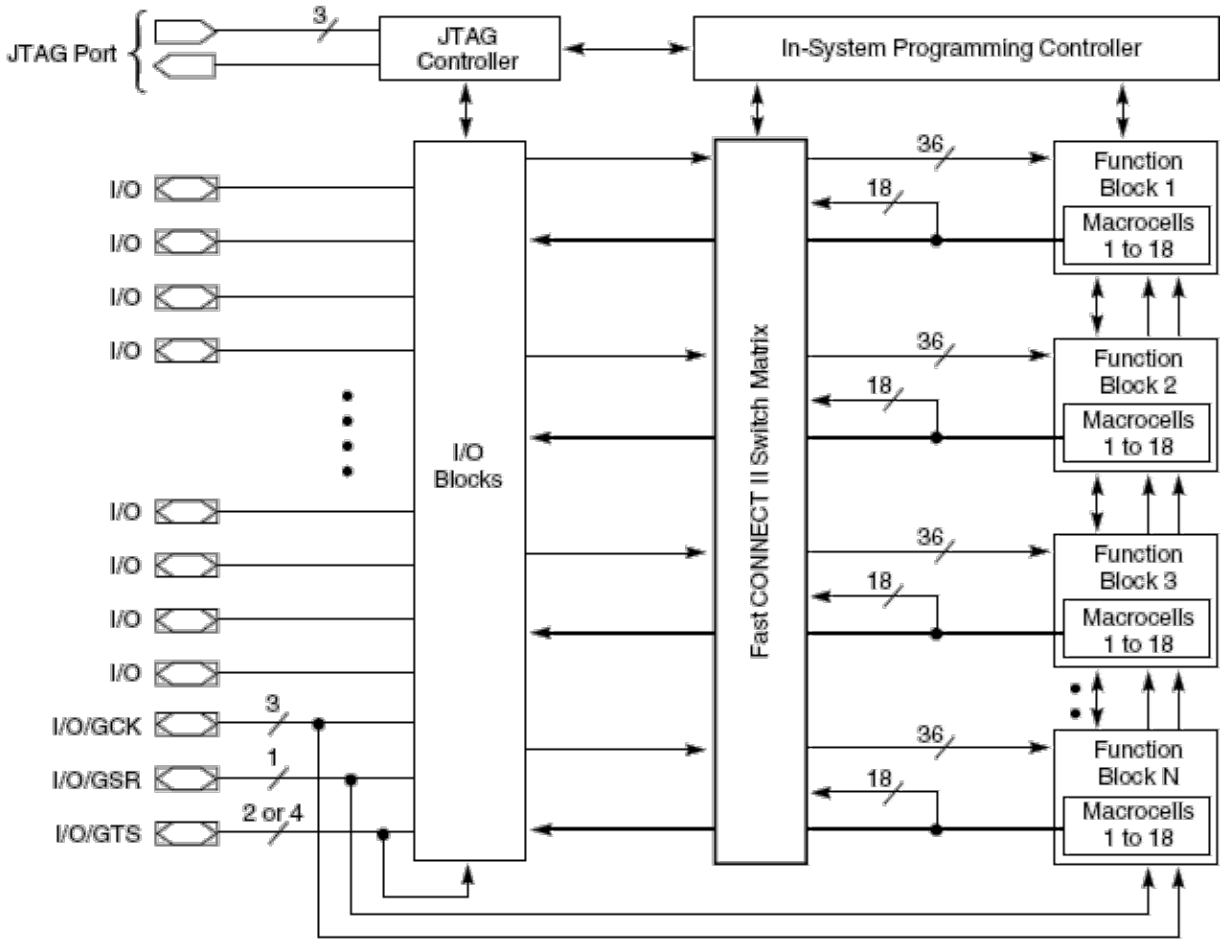
FPGA: evolution

- PAL: Programmable Array Logic
  - End of 1970s
  - Canonical form
  - Programmable input, fixed output
    - Less programmed connections: faster signal propagation
  - Method of programming
    - OTP: one time programmable
    - Erasable: using UV light
    - Flash kofiguration
  - Advancement: PAL can be configured not only during production but also by developper
- Advanced version: GAL (Generic Array Logic)
  - Larger complexity, can substitute more PAL device
  - Reconfigurable
  - Adequate for prototyping



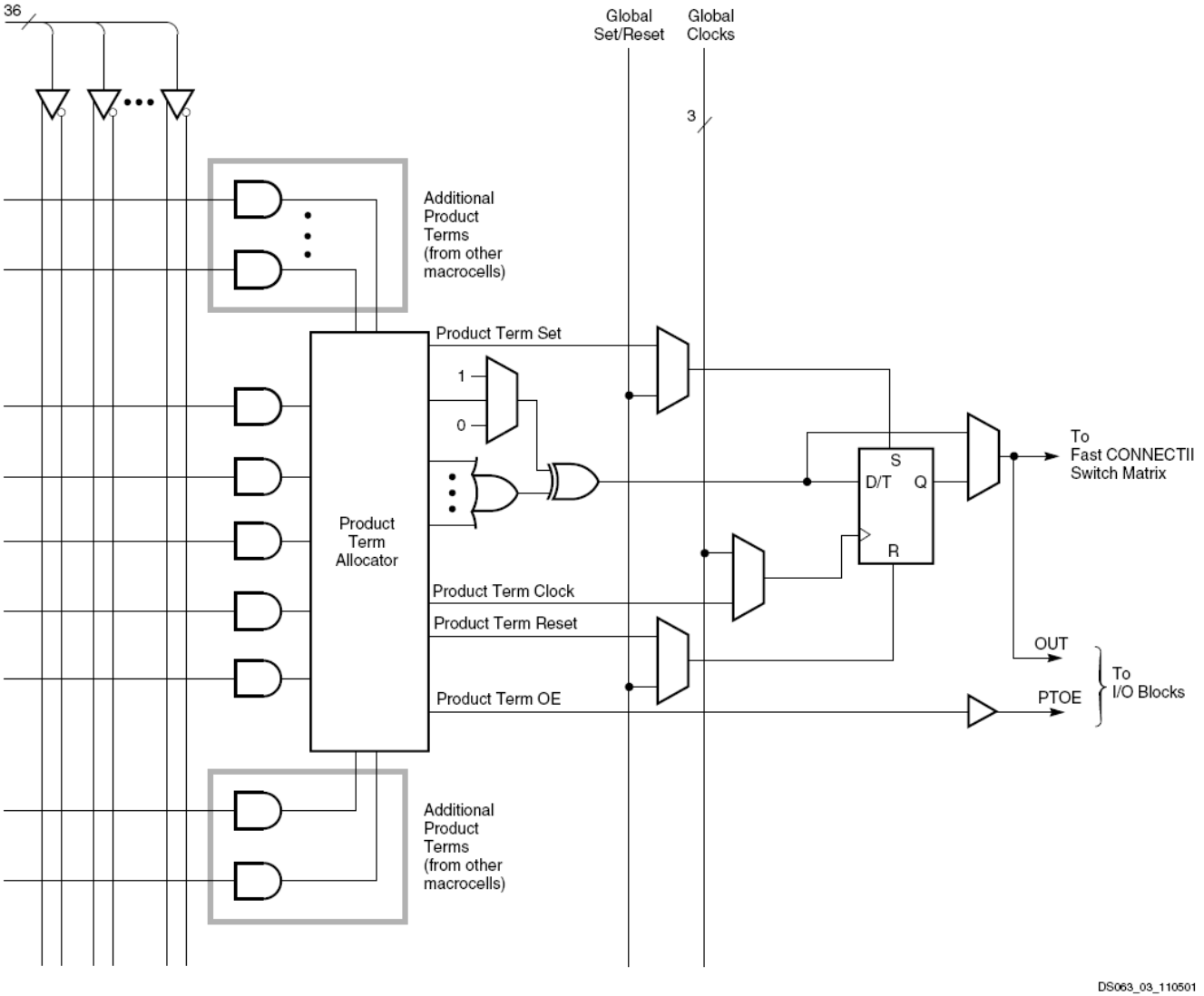
FPGA: evolution

- CPLD (Complex Programmable Logic Devices)
- Comlexity: between PAL and GAL
- Architecture:
  - Function block
  - Macrocell
  - Wiring matrix
- Function block: contains macrocell
- Macrocell: multiple-input single-output logic function (combinational or register output)
  - Architecture is similar to PAL



CPLD macrocell

- Architecture of a macrocell: canonical implementation of logic functions

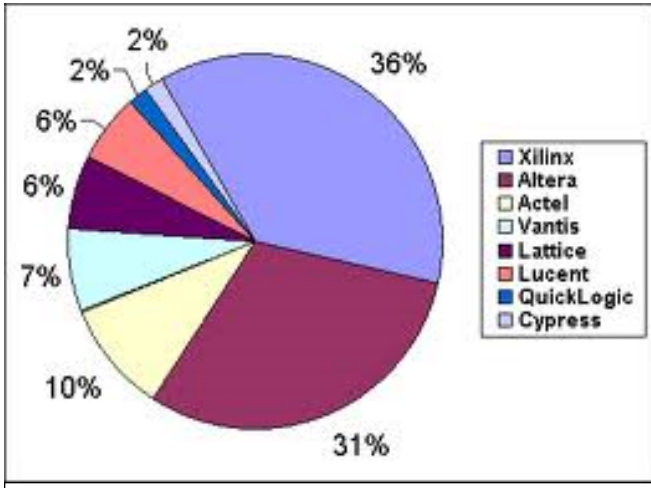


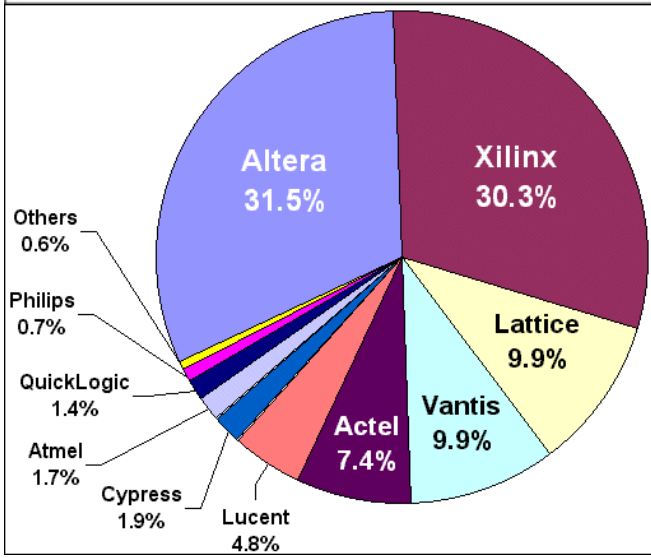
FPGA: evolution

- FPGA: Field Programmable Gate Array
- High-complexity device
- Not necessarily follows the canonical structure
- Several auxiliary components are found
  - Clock-management
  - Flexible configurable IO block
  - Embedded RAM
  - Multiplier

FPGA manufacturers

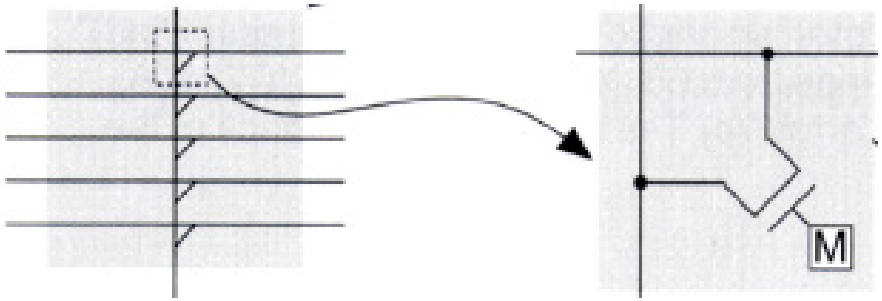
- Some larger manufacturer:
  - **Xilinx**
  - **Altera**
  - Actel
  - Vantis
  - Lattice
  - Lucent
  - QuickLogic
  - Cypress
  - Atmel
- In the followings Xilinx products are used to learn about FPGAs

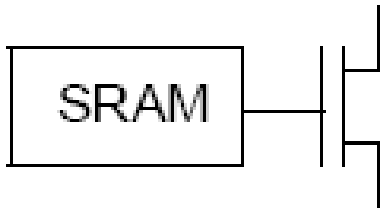




Storing the configuration

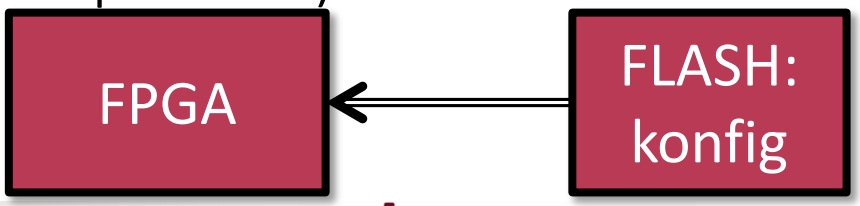
- Configuration file: contains the internal connections
- NOT A PROGRAM
  - Word ‘programming’ mainly refers to downloading the program but in case of FPGA not a program is written instead it is configured how the HW should work (behave)
  - The configuration is quite complex and really seems to be a program but it is not a program
- Configuration: making connections between data lines





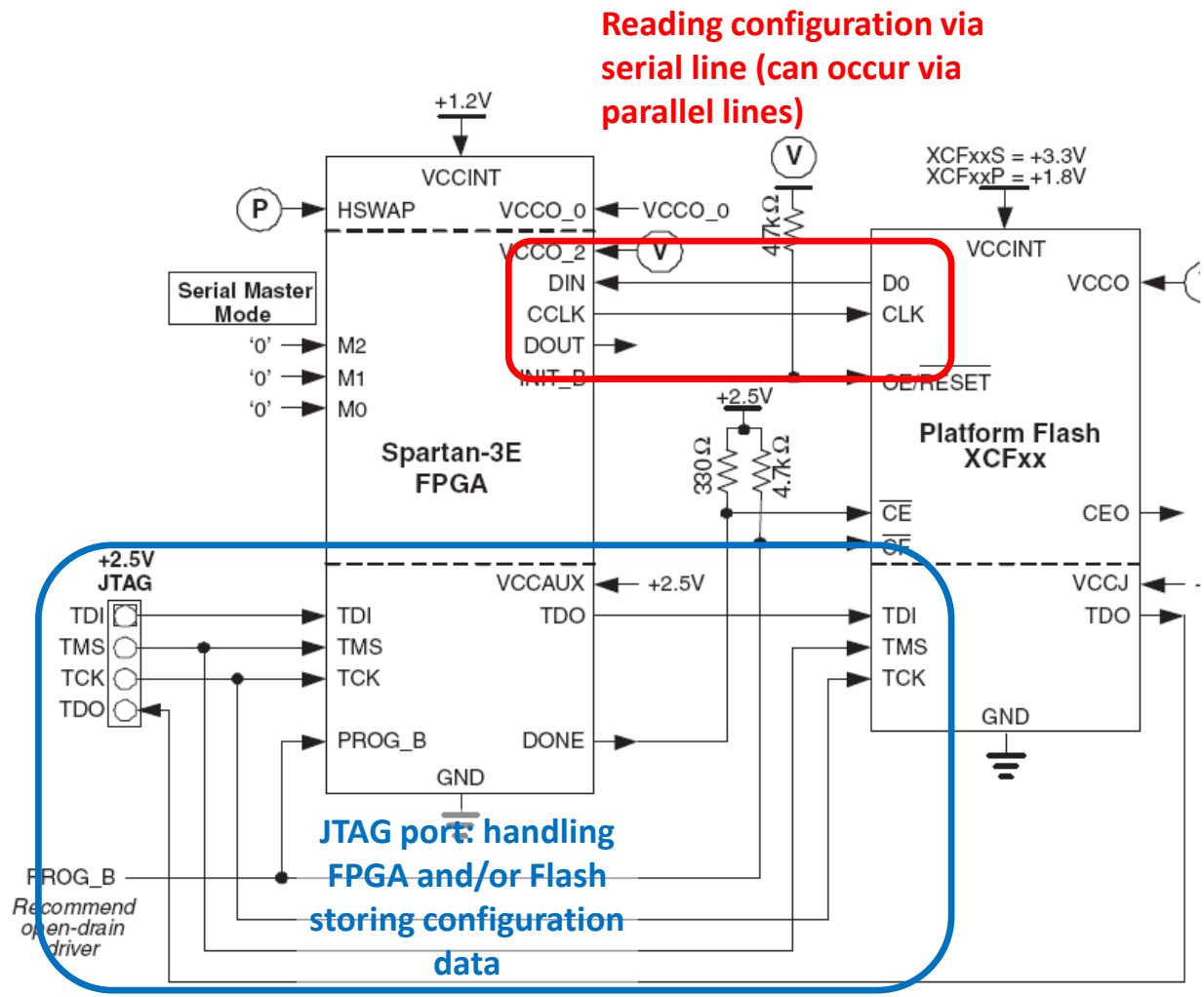
Storing the configuration

- Reading method of configuration (serial, parallel, JTAG) can be set using external wires
- In FPGAs the configuration data (e.g. connections in a switching matrix) is loaded into an internal SRAM
- Flash-based FPGAs are quite rare now
  - SRAM-based configuration allows larger component density ☺
  - During operation can be reconfigured even partly ☺
  - Booting delay of the system is larger: configuration must be loaded into the internal SRAM cells ☹
- Loading configuration: during booting it occurs from external Flash memory or a host PC
- There exist FPGAs containing internal Flash but even in this case booting delay of configuration is inevitable. Their advantage is the smaller area requirement compared to FPGA+Flash and more secure since the configuration process cannot be seen (reverse engineering can be prevented)



Storing the configuration

- FPGAs are reconfigurable during development via a standardized JTAG interface
- JTAG port can be used in a daisy chain toward other devices
- JTAG can be used for writing the external Flash that stores the configuration
- The configuration is stored in the Flash and read from Flash later at FPGA booting

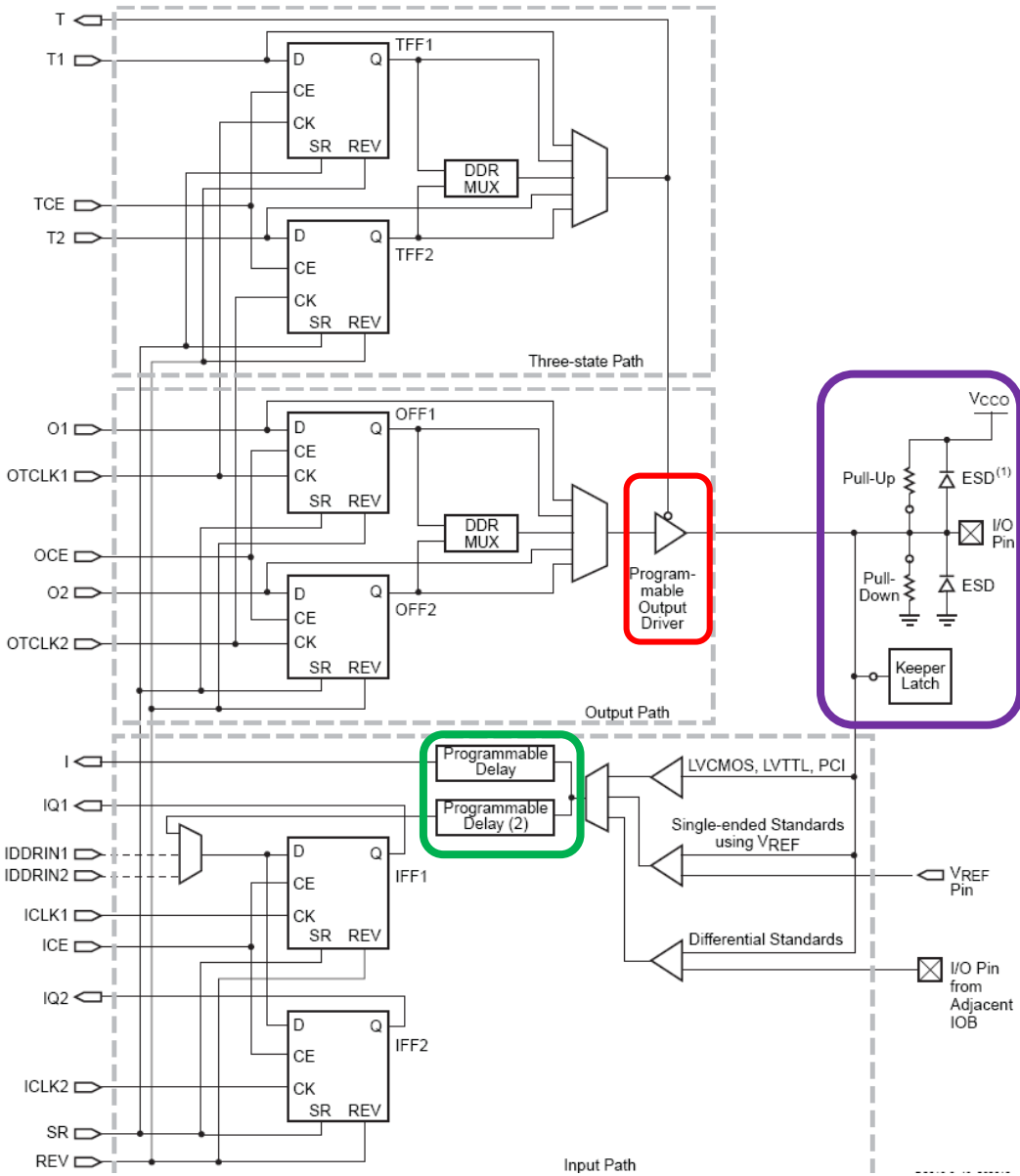


Input-Output blocks in FPGA

- Flexible configurable Input-Output (IO) block
- Three main signal lines:
  - Output drive
  - Input lines
  - Output lines

Input-Output blocks in FPGA

- Programmable input/output setting (see: Programmable Output Driver)
- Programmable pull-up or pull-down resistances
- Keeper latch: can be set that the last value is kept in high-impedance mode and not allow the level floating
- Internal delay lines: input signals are fed directly into the FPGA, the clock signal however get to the IO block via the internal clock division unit and suffers from delay: forcing delay to the data input it can be synchronized with the CLK
  - Delay is dynamical, can be configured even during operation



Input-Output blocks in FPGA

- DDR: Dual-Data-Rate Transmission: data rate is doubled when data transmission occurs for both the rising- and falling edge of the CLK
  - D flip-flops used in the conventional manner (triggered for only rising CLK edge) but their CLK signal is designed in a special way:
    - 180° phase shift
    - inverting
  - Writing is done alternately: once into one FF, then into the other FF