Analog to Digital Converters

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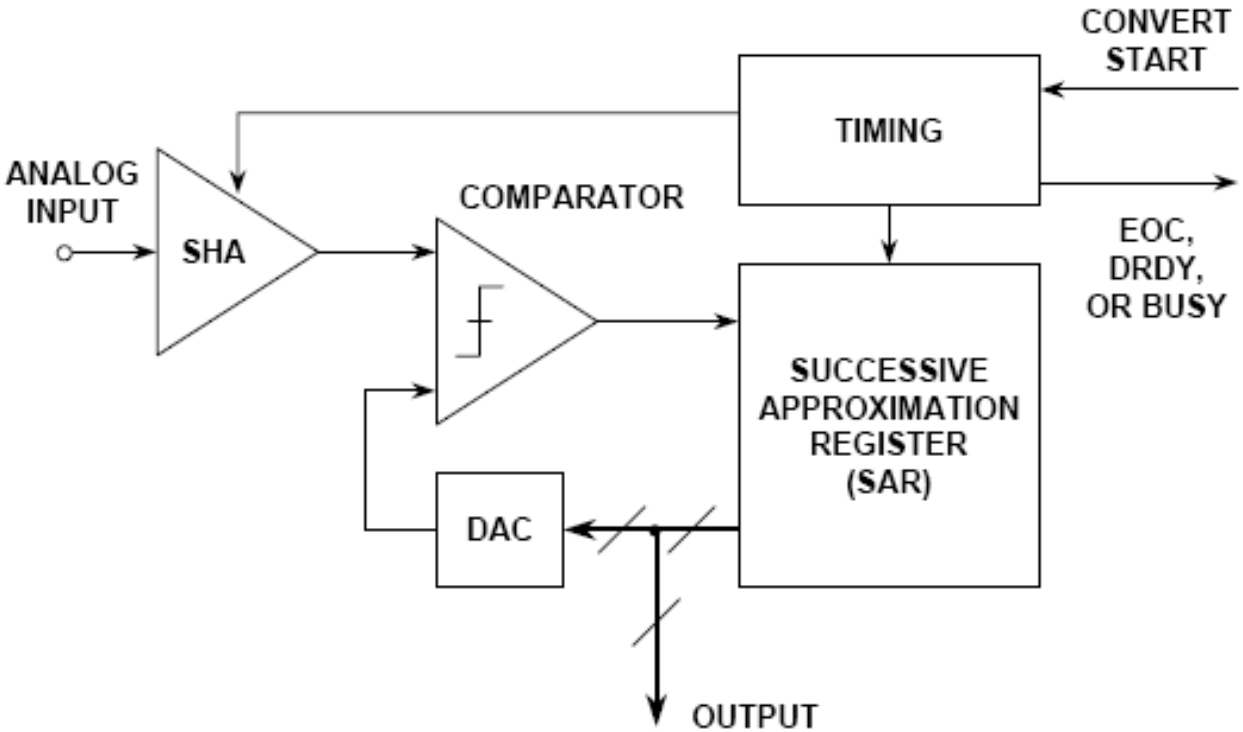
ADCs in general

- Mode of conversion
  - Direct: measured voltage is directly converted into a digital signal (feedbacked or not)
  - Indirect: measured voltage is converted into time, frequency, etc., first then into digital signal
- Mode of measurement
  - Instantaneous value: at difened time instants
  - Average value: at amplitude dependent time instant

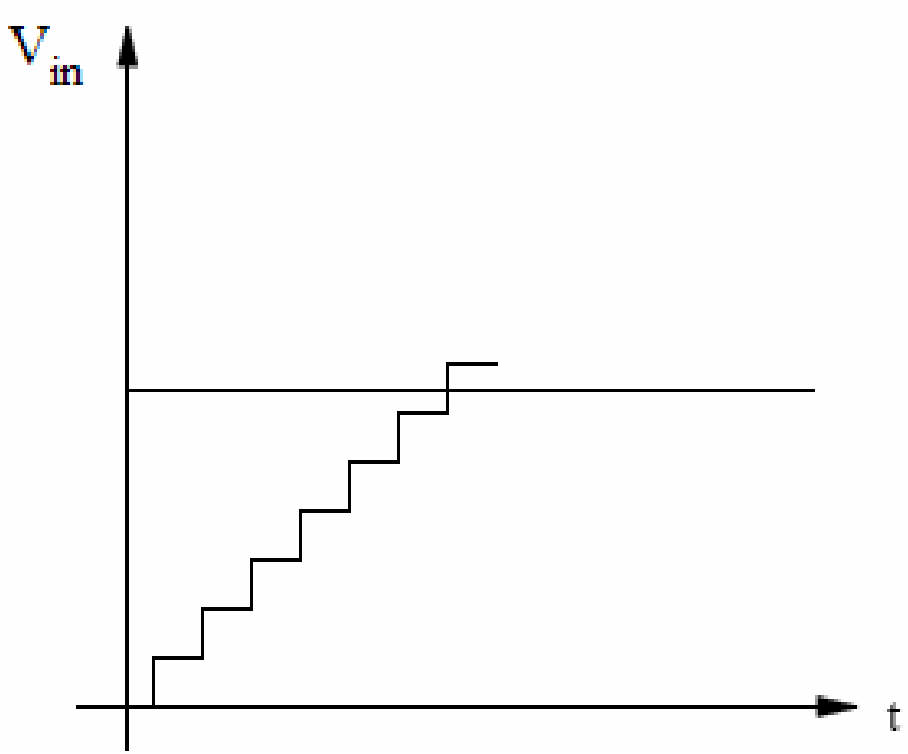
Successive approximating ADC

- An example for ADC with feedback

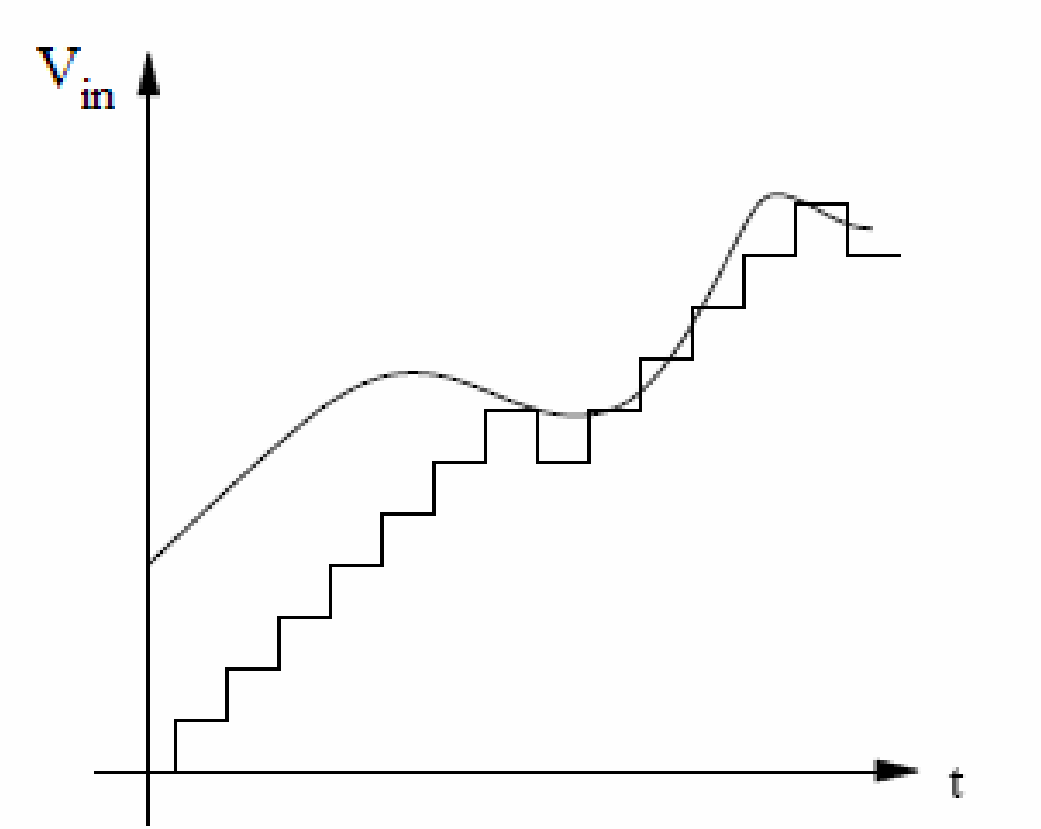


- Accuracy and lineraity of the ADC is determined by the DAC unit
  - DAC remark:
    - in the past laser trimmered thin-film resistors were used->expensive and vulnerable
    - Today switched capacitorr are used->great teperature tracking <1ppm/Celsius

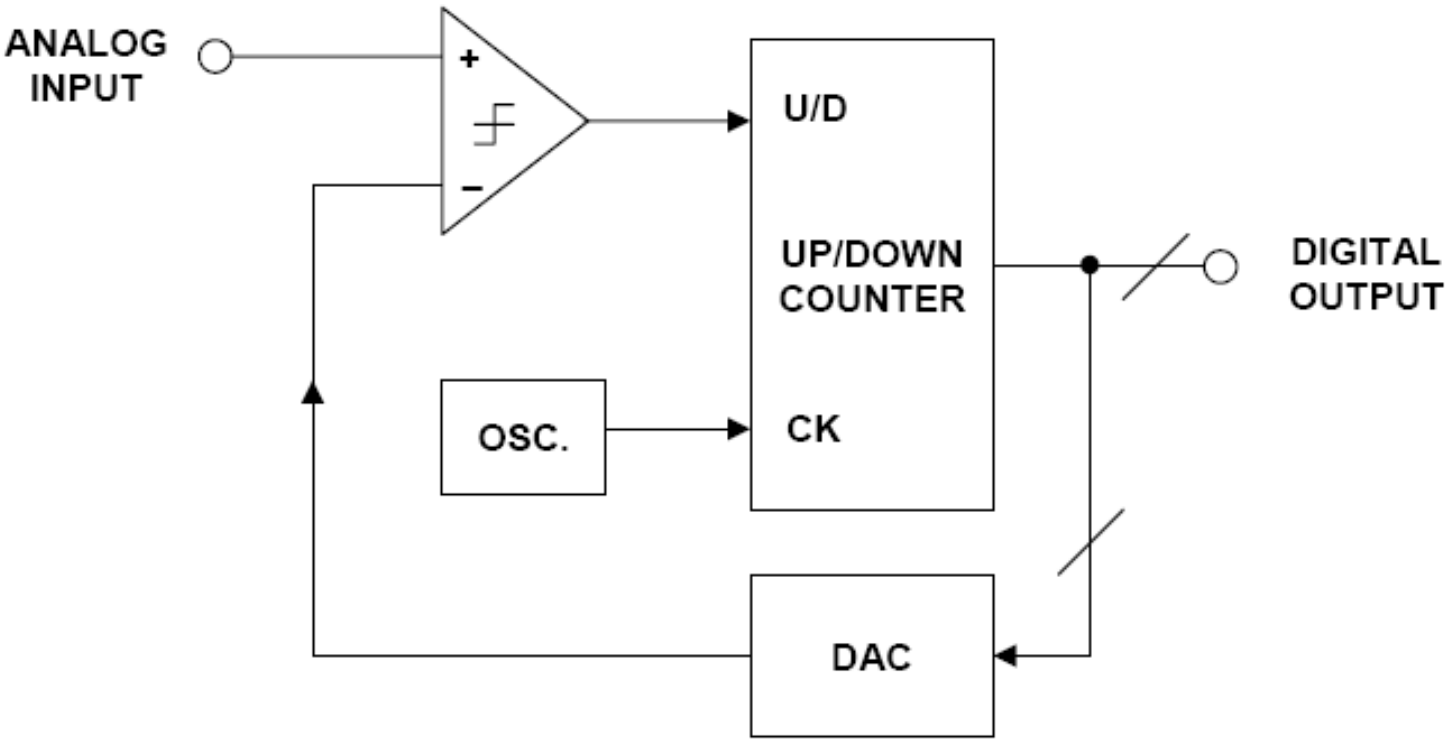
- Control solutions:
  - ADC with counter: very slow
    when level reached,
    it is grabbed



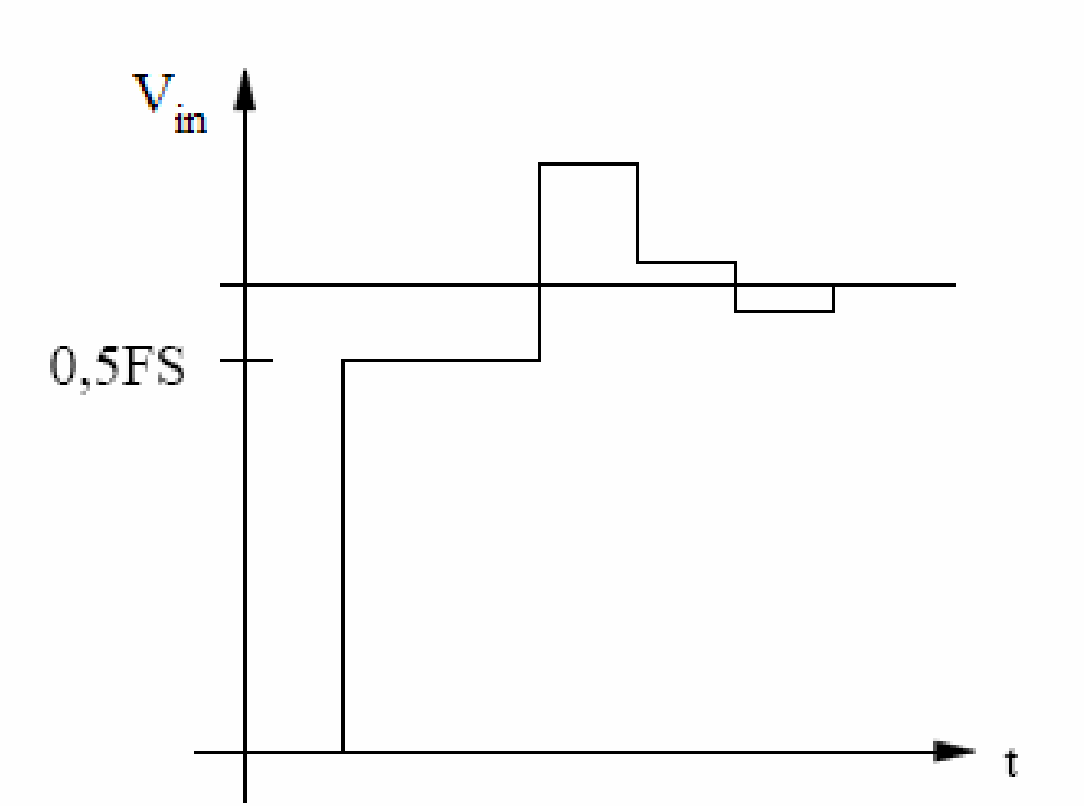
– Tracking counter: slow
when level reached,
it is tracked



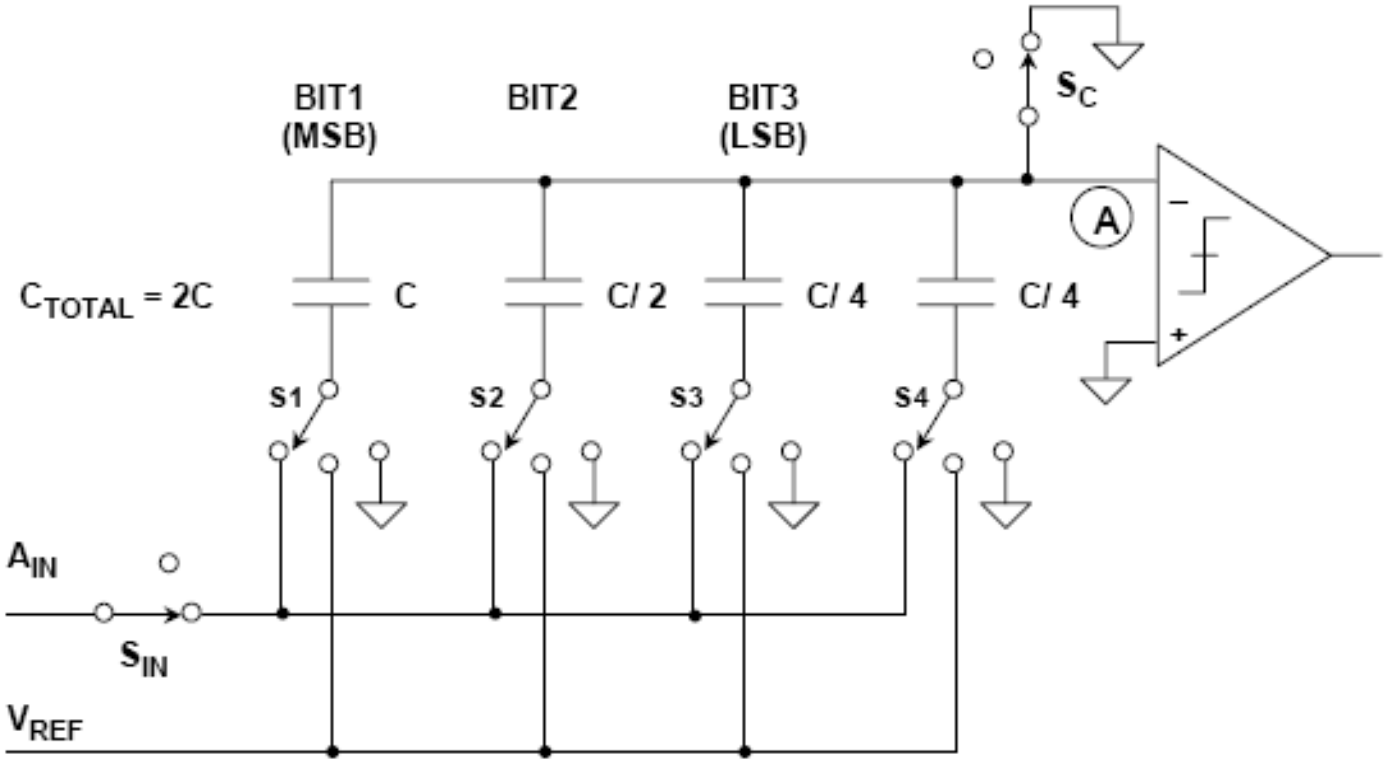
- Block diagram:



– Successive approximating: most popular
12-16 bits



Switched capacitor DAC

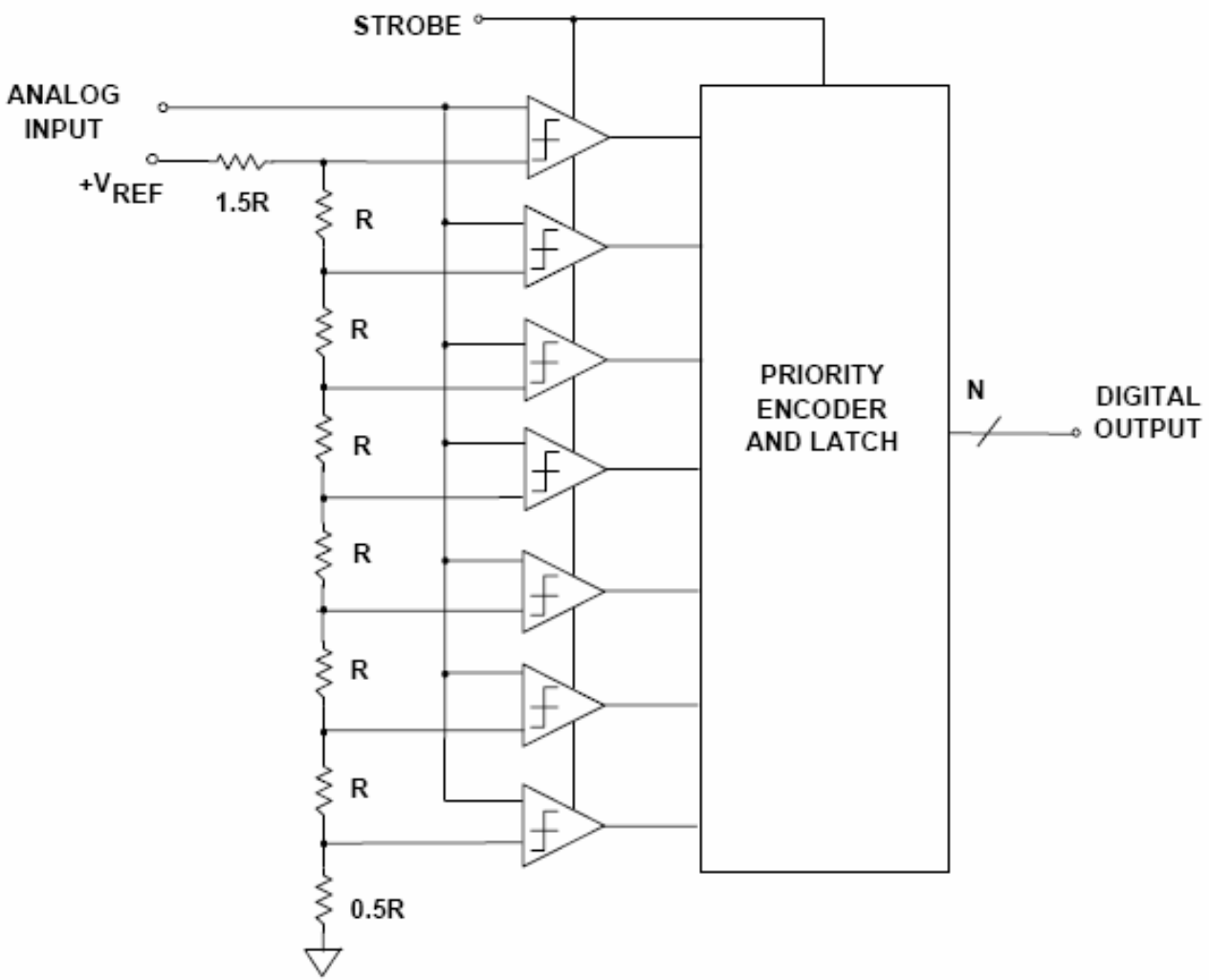


- S_{in}, S_C on: track or sample
- S_{in} off: hold
- S_C off: node A moves as the bit switches are manipulated

- S_1 S_2 S_3 S_4 grounded: $V_A = -A_{in}$
- S_1 switched to V_{REF}: $U_A = V_{REF}/2 - A_{in}$

- Note: sum of C=2C all the time (C=Q/V)

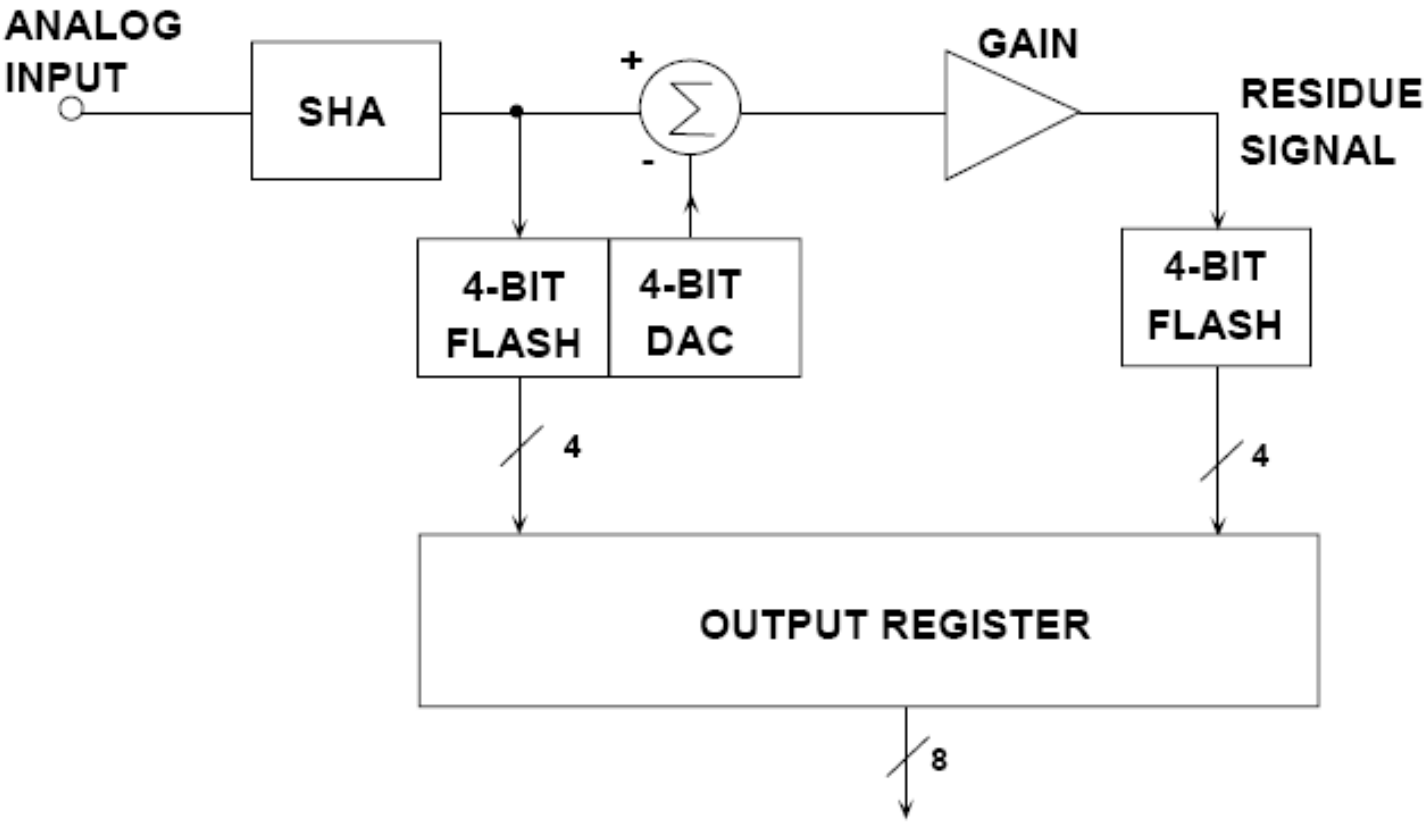
Falsh converter (parallel ADC)



- For N bit resolution:
  - 2^N resistors and
  - 2^N-1 capacitors are needed
- Features:
  - Too many resistors
  - Big Si area
  - Expensive
  - Laser trimmering
  - High input capacitance
  - Poor linearity
  - Fast: 100MHz->10-12bit; 1-20GHz->8bit

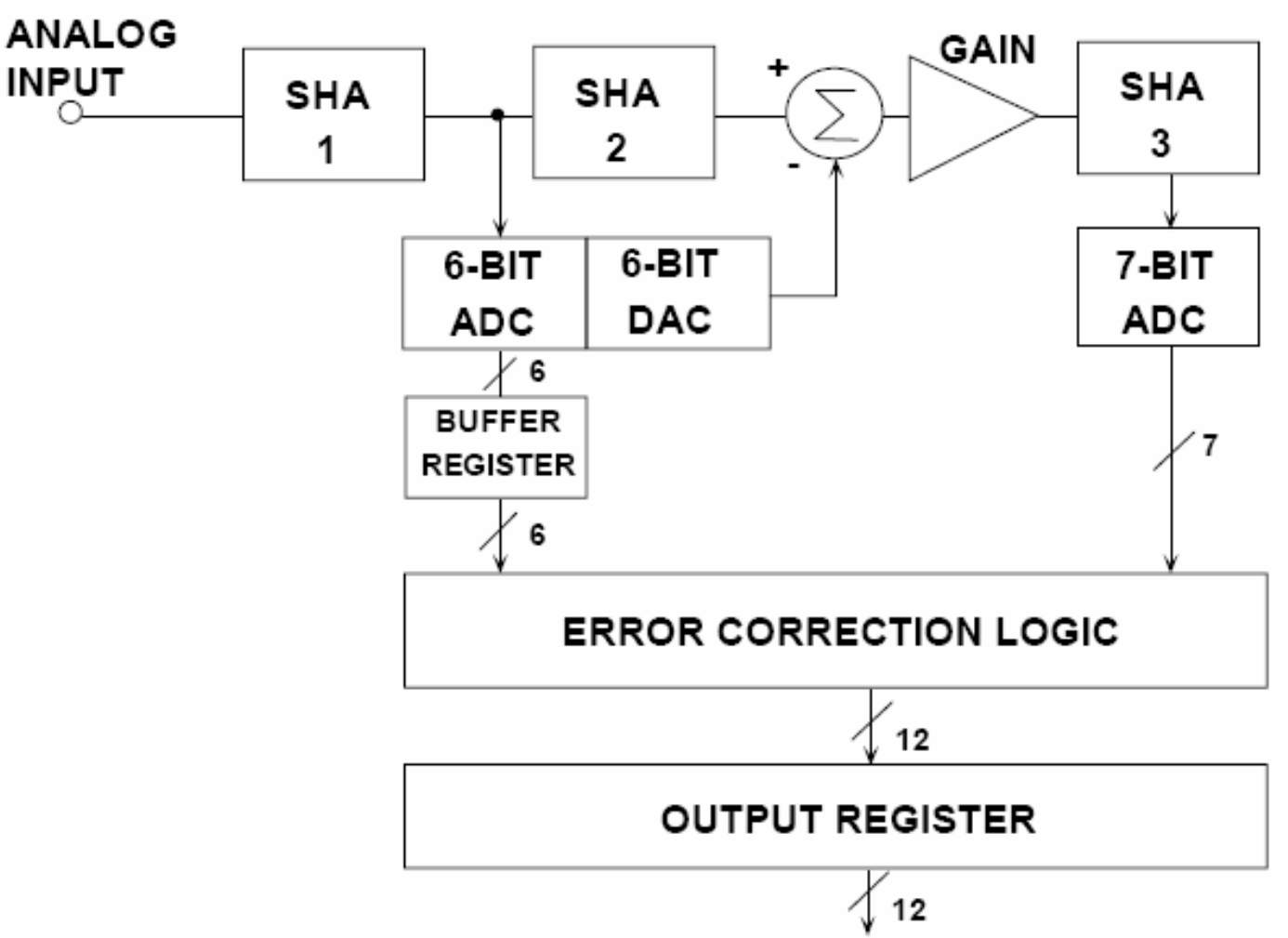
Subranging ADCs

- Flash advantages without disadvantages



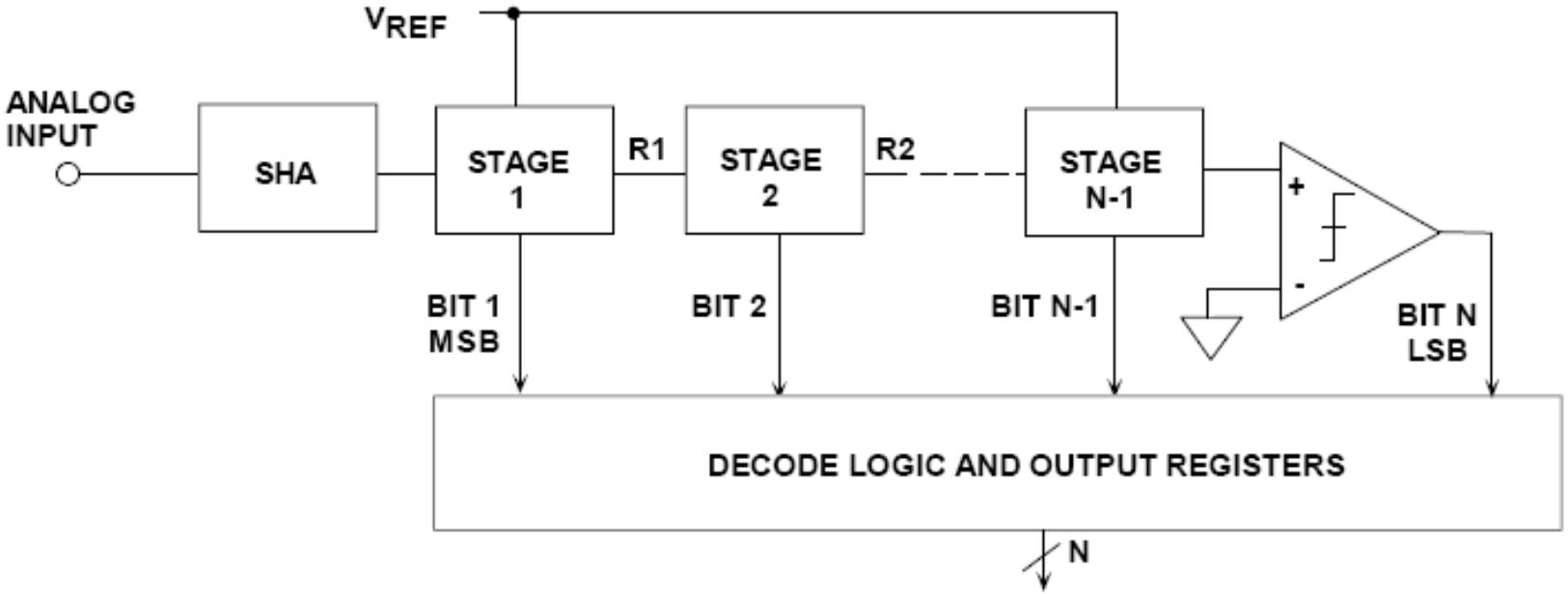
- Lower power consumption compared to Flash AD
- Smaller Si area
- Less resistors of one order is needed than in case of Flash AD
- ½ speed reduction compared to Flash AD
- How to speed up: use pipeline technique

Pipelined subranging ADC

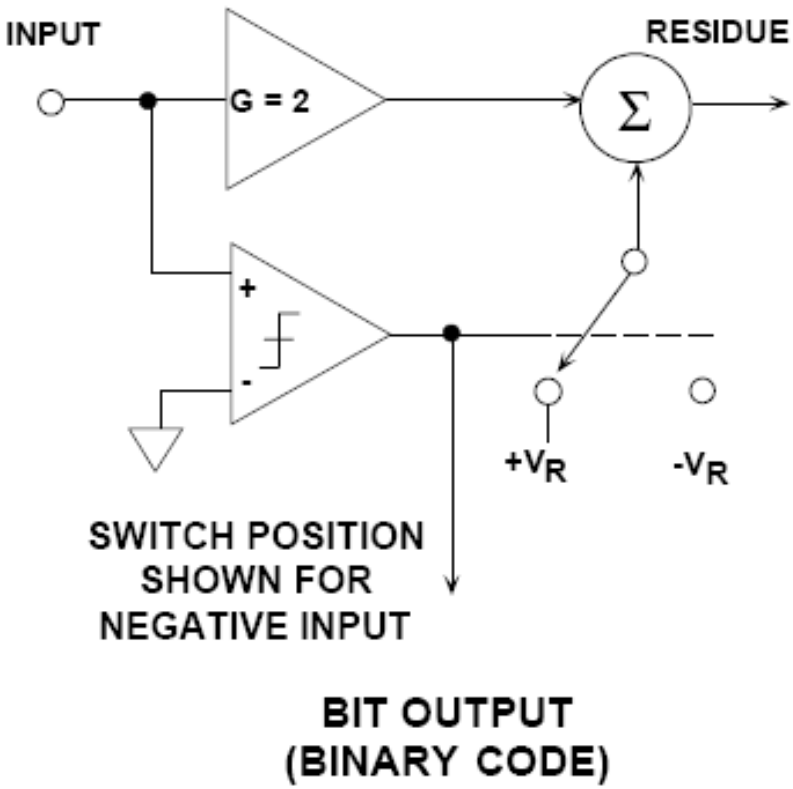


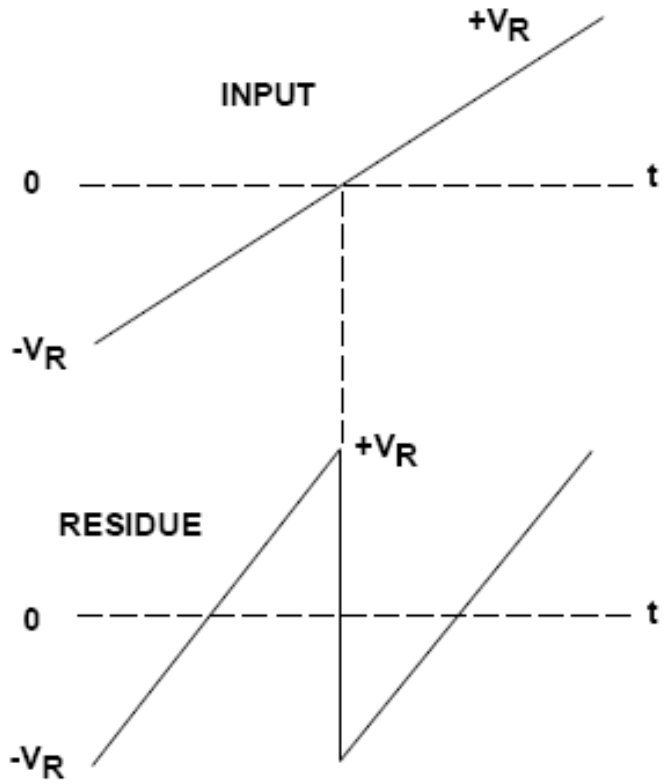
Bit-per-stage ADC (serial, ripple)

- One form of multistage subranging ADC with one bit per stage and no ewrror correction

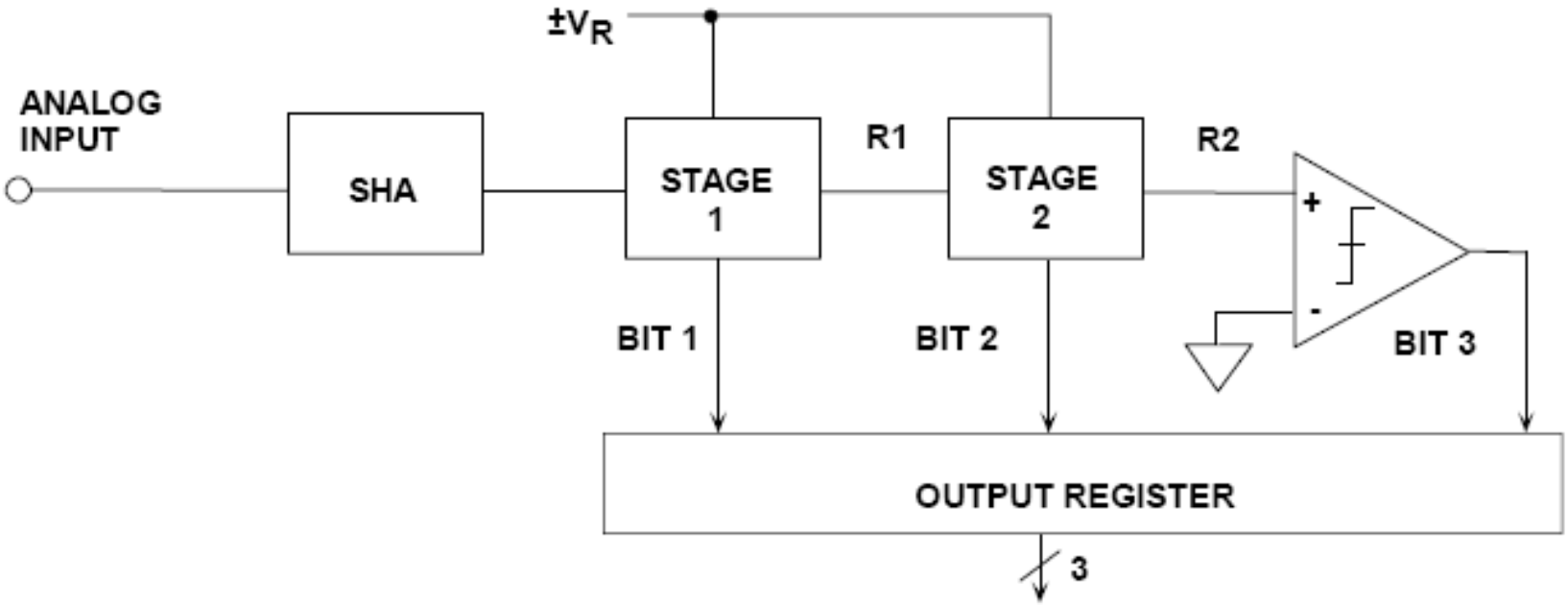


- Simple stage of binary DAC

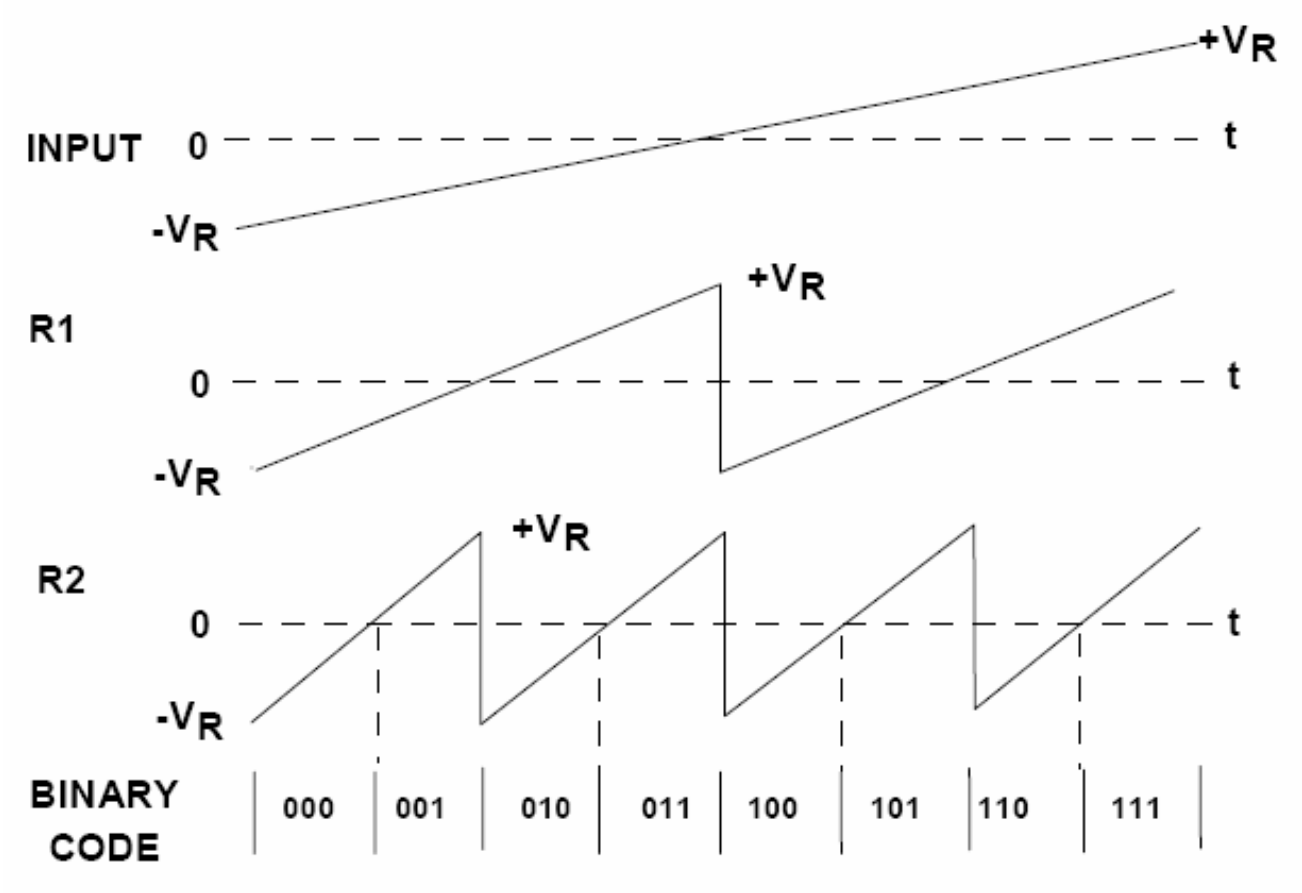




- 3-bit case:

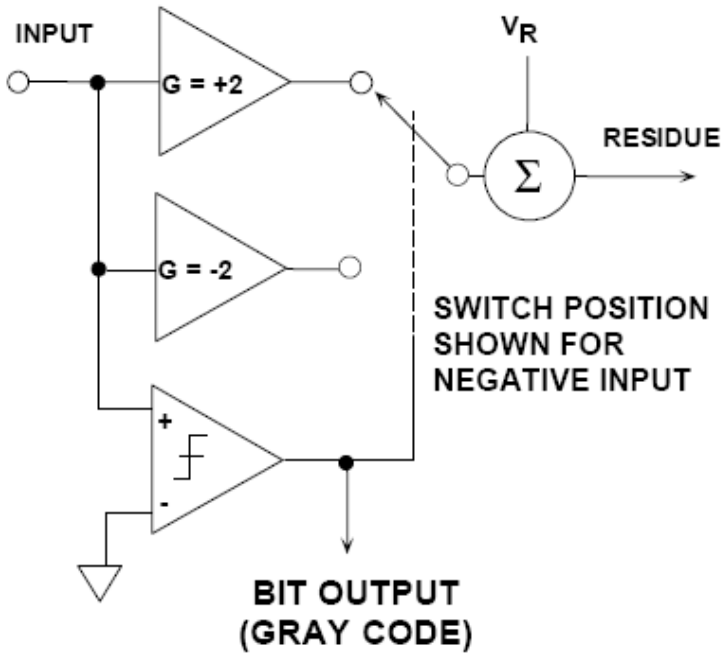

±V_R
ANALOG INPUT
SHA
STAGE 1
R1
STAGE 2
R2
+
-
BIT 1
BIT 2
BIT 3
OUTPUT REGISTER
3

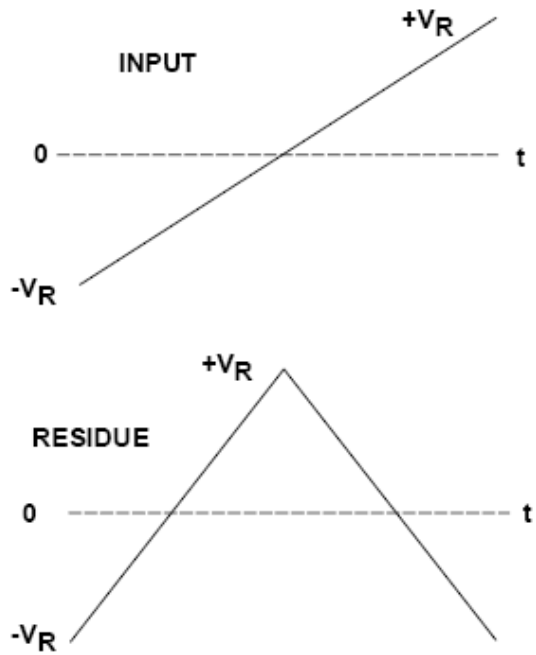
– Input and resdue wavefroms
  - See and understand using the simulation SW



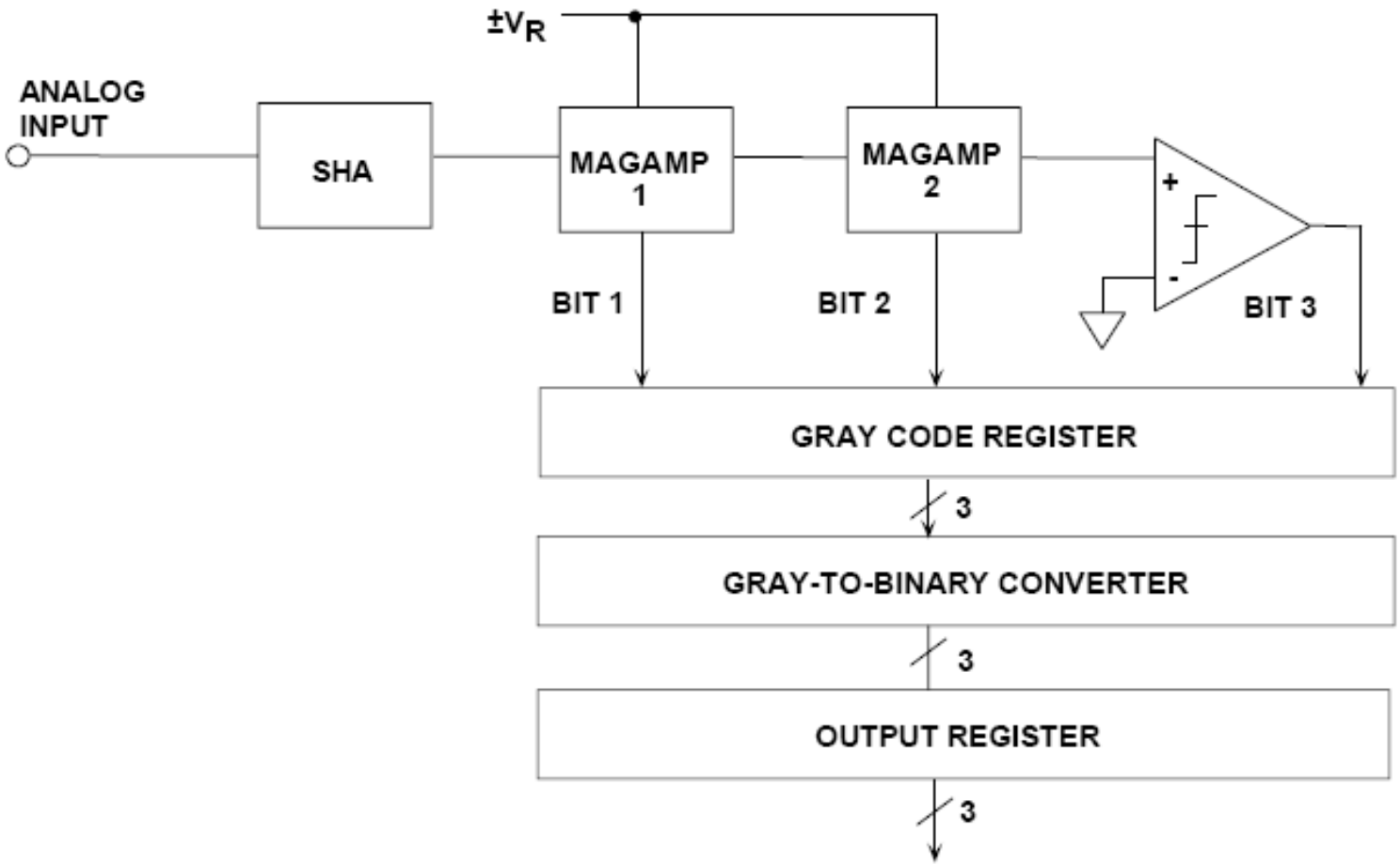
- Input is a ramp signal
- Long settling time because of discontinuities
- Note: R2 has 2x frequency compared to R1

- Magnitude amplifier is a better architecture

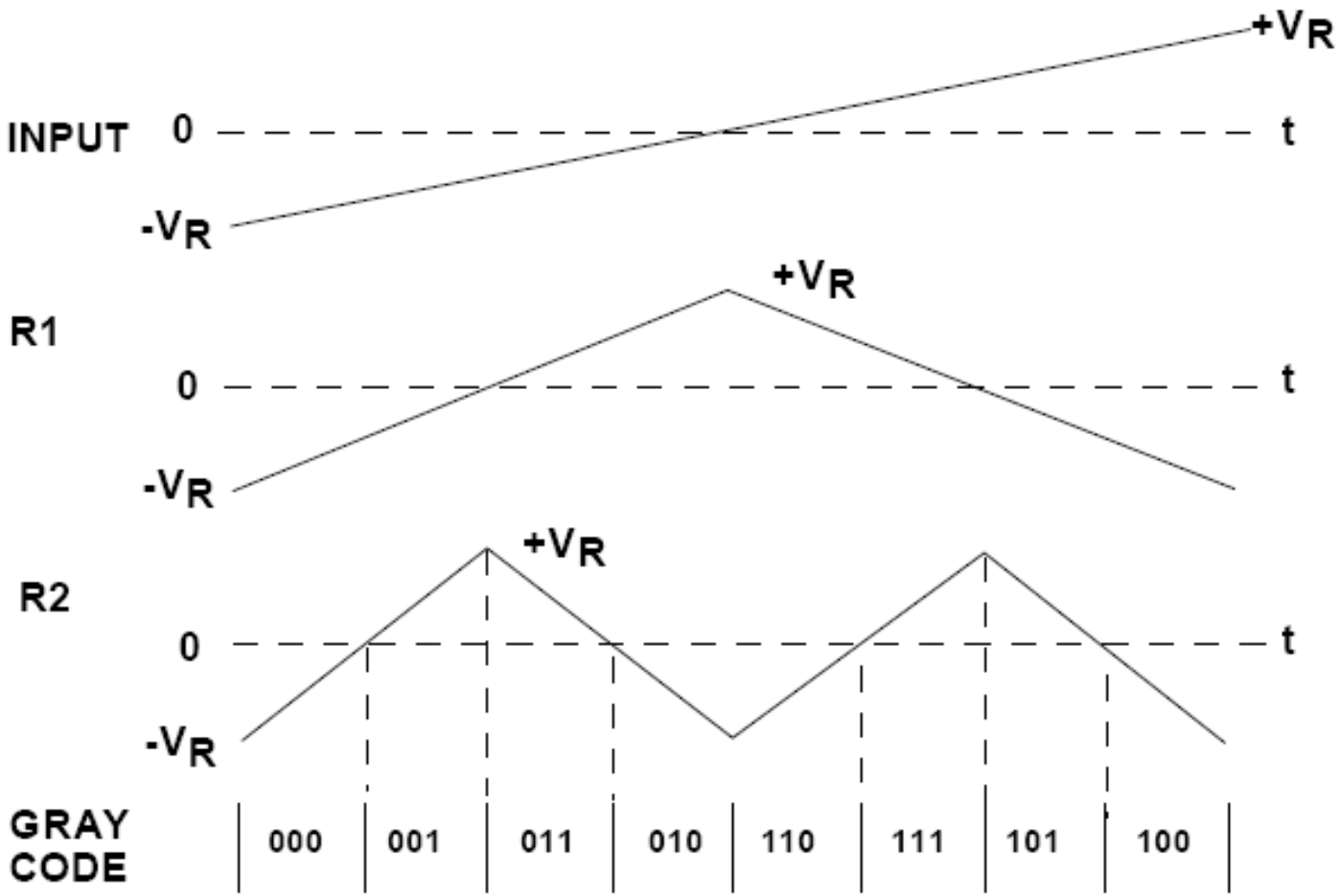




– MagAmp block diagram



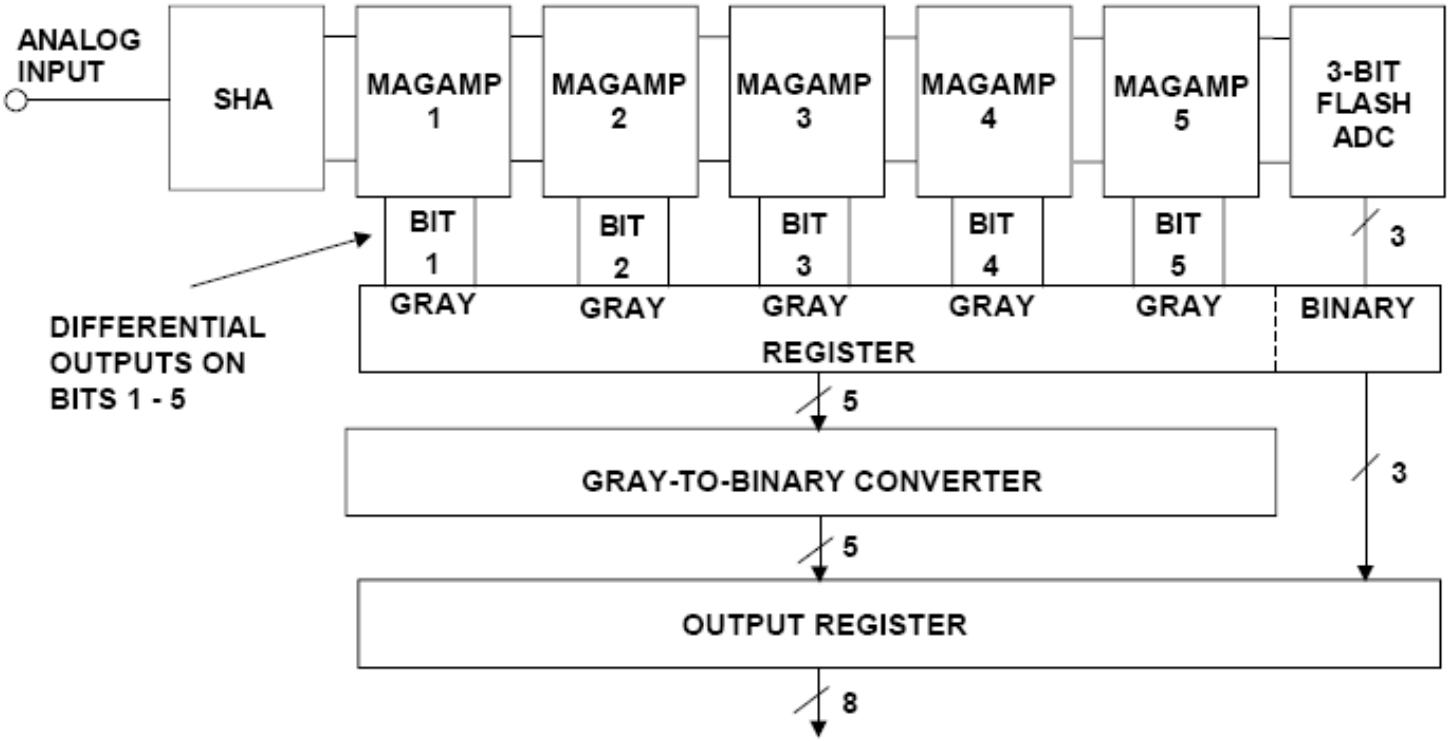
– Input and residue waveforms



- No discontinuity
  - Fast settling
  - High speed->competitor to Flash AD
- No meed for laser trimmered resistances
- Note: outputs Gray-code that has to be converted into standard binary

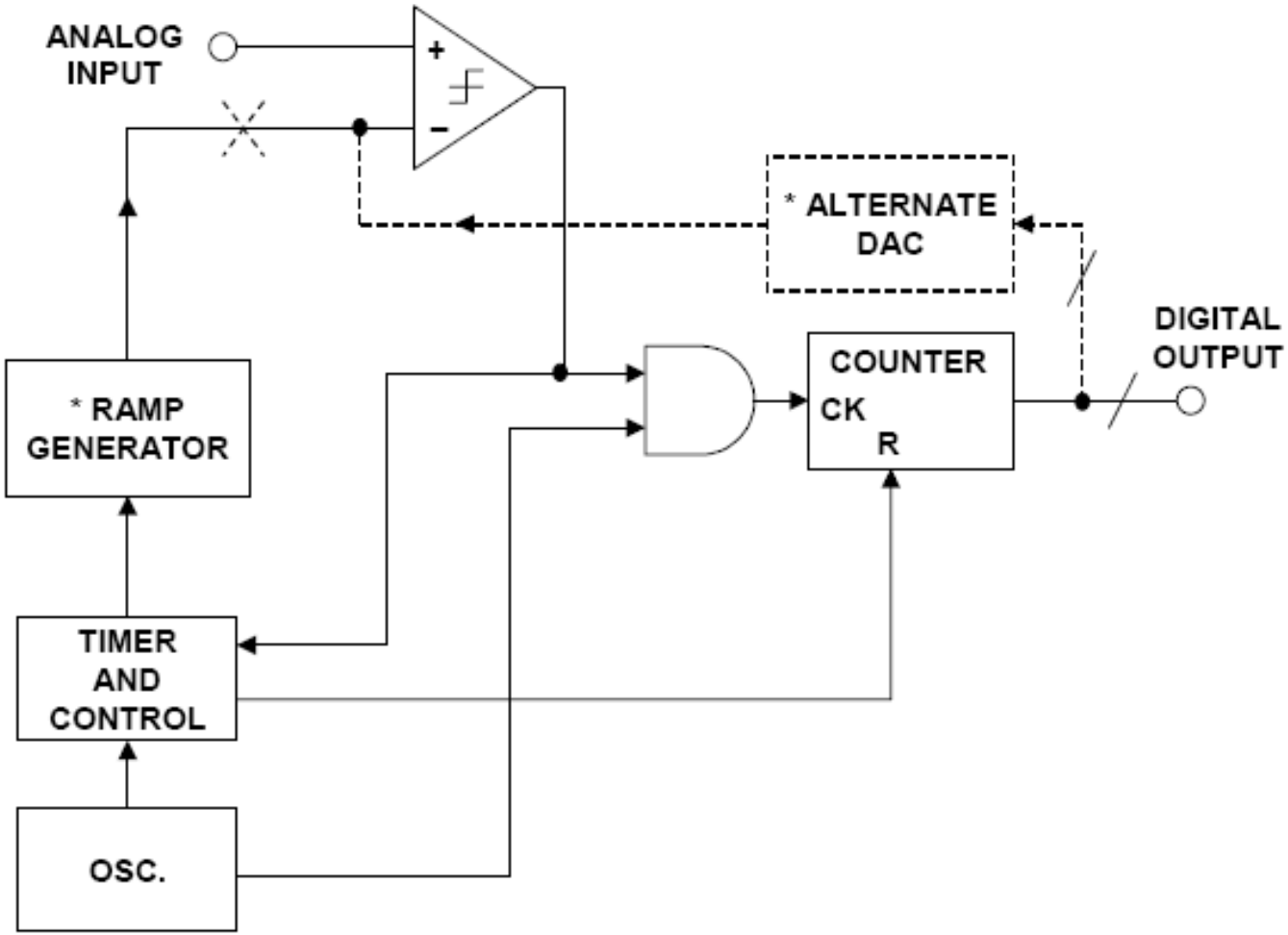
Dual architecture

- Example: first 5 bits MagAmp last 3 bits Flash



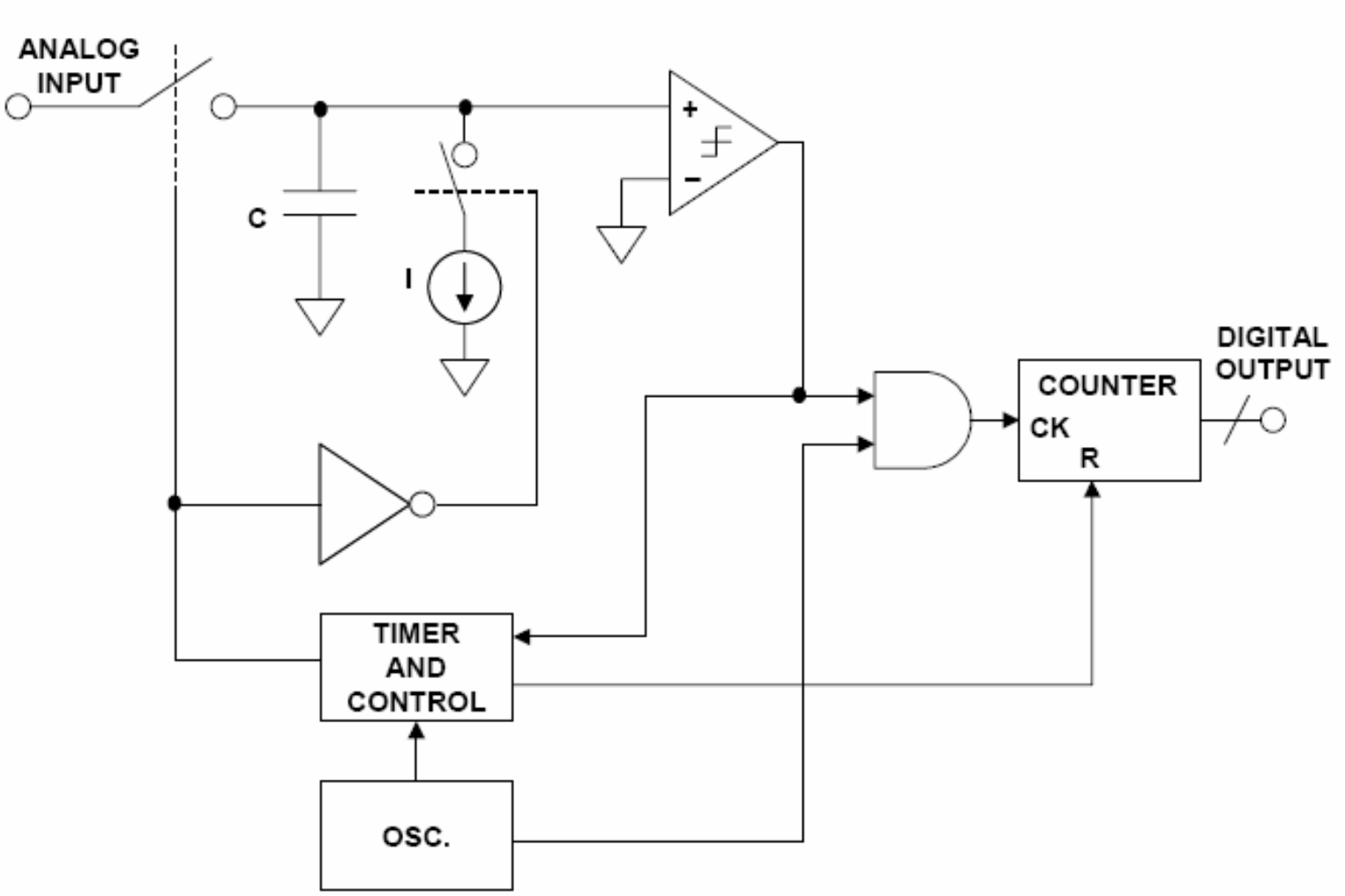
– Resolution: 8-bit
– Speed: 100 MSPS

Ramp Run-Up ADC



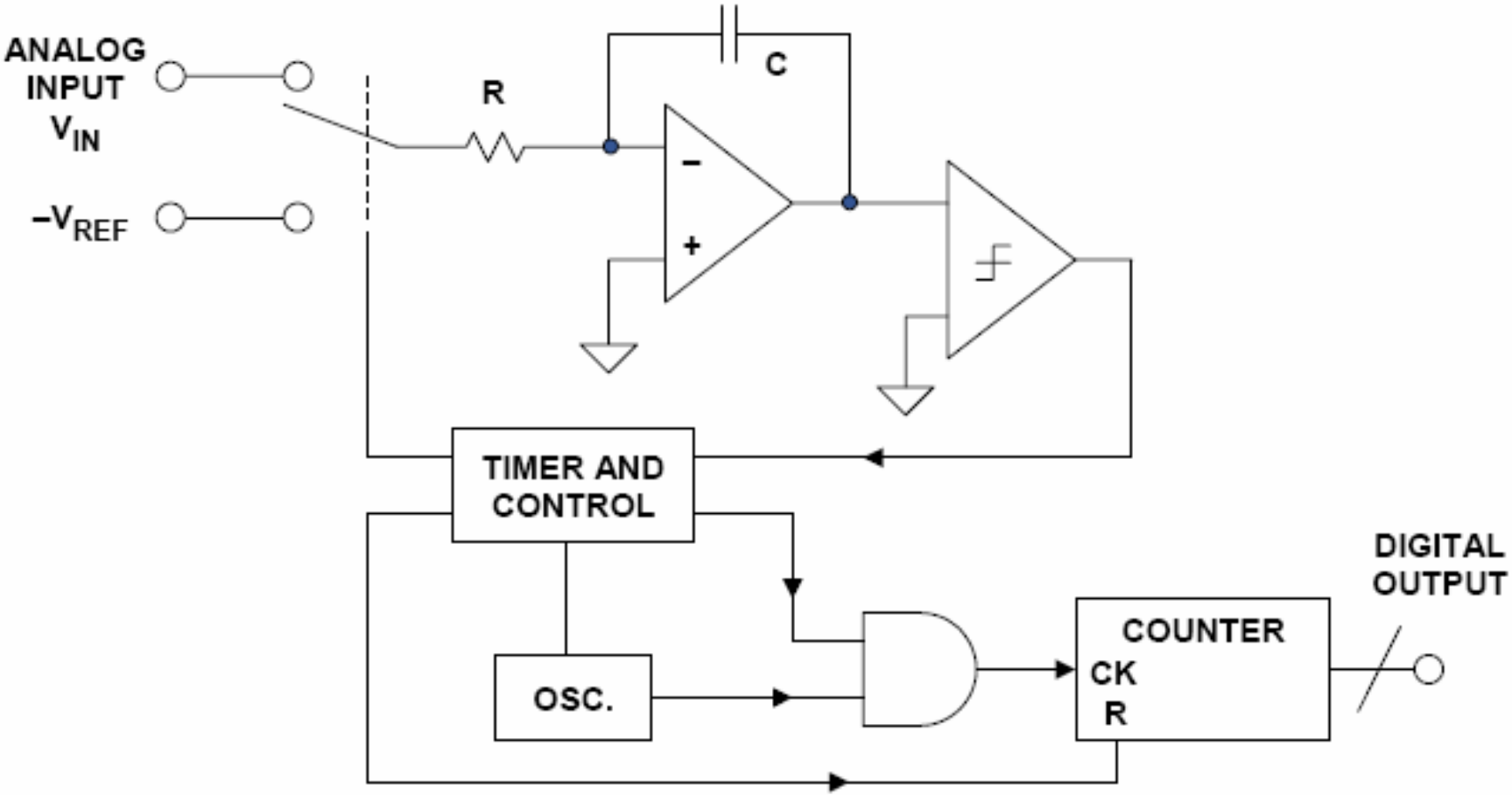
- Indirect measurement
  - Voltage->Time->Digital output
  - Instantaneous value
- Counter registers the oscillator ticks
- Sampling at the end of the conversion
- Amplitude dependent sampling
  - Should be eliminated: use charge run-down architecture

Charge Run-Down ADC

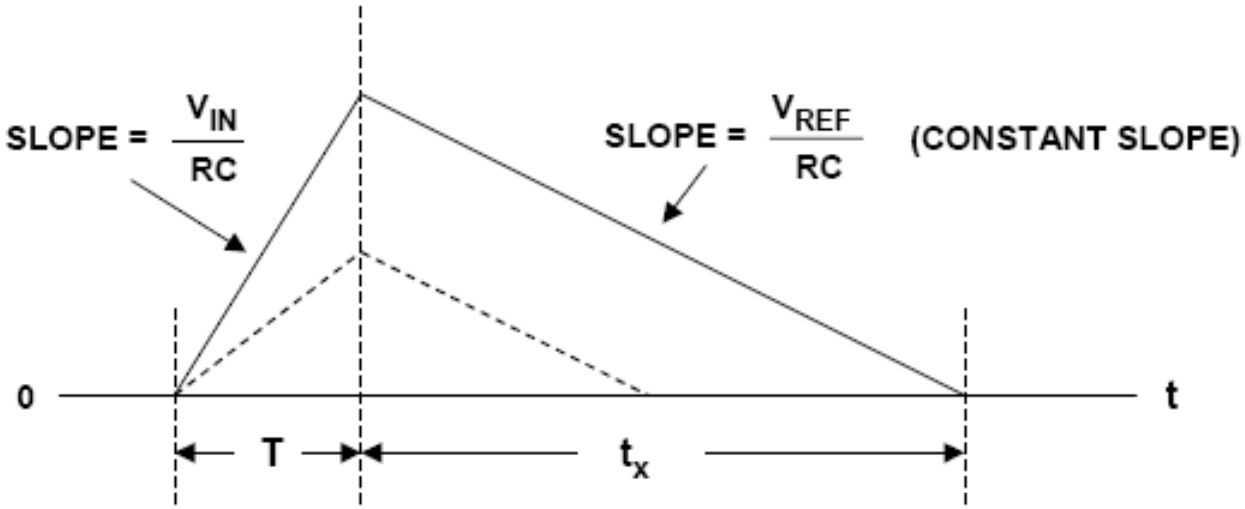


- Capacitor is charged up to the input voltage
- Counter measures the discharge time of capacitor caused by current source
- Accuracy is determined by:
  - Value of capacitance
  - Amplitude of current
  - Time base
- Sampling starts at power on

Dual Slope ADC



- Integrator output waveforms



$$\frac{V_{IN}}{RC} T = \frac{V_{REF}}{RC} t_x$$

$$t_x = \frac{V_{IN}}{V_{REF}} T$$

- Only a short time stability is needed for the clock generator
- Reference voltage dependent

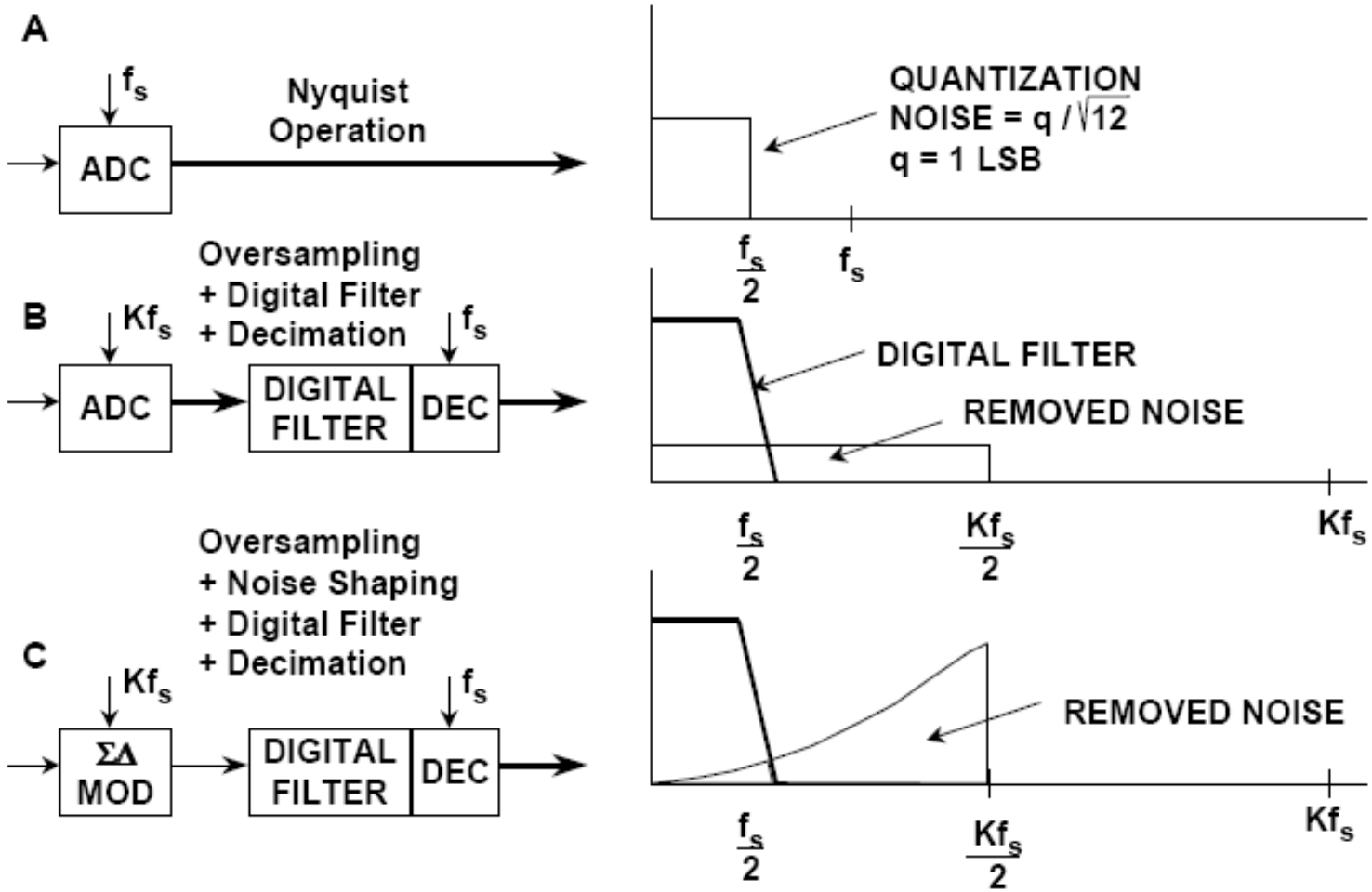
Voltage-to-Frequency ADC

– monotonic
– free of missing codes
– Integrates noise
– consume small power.

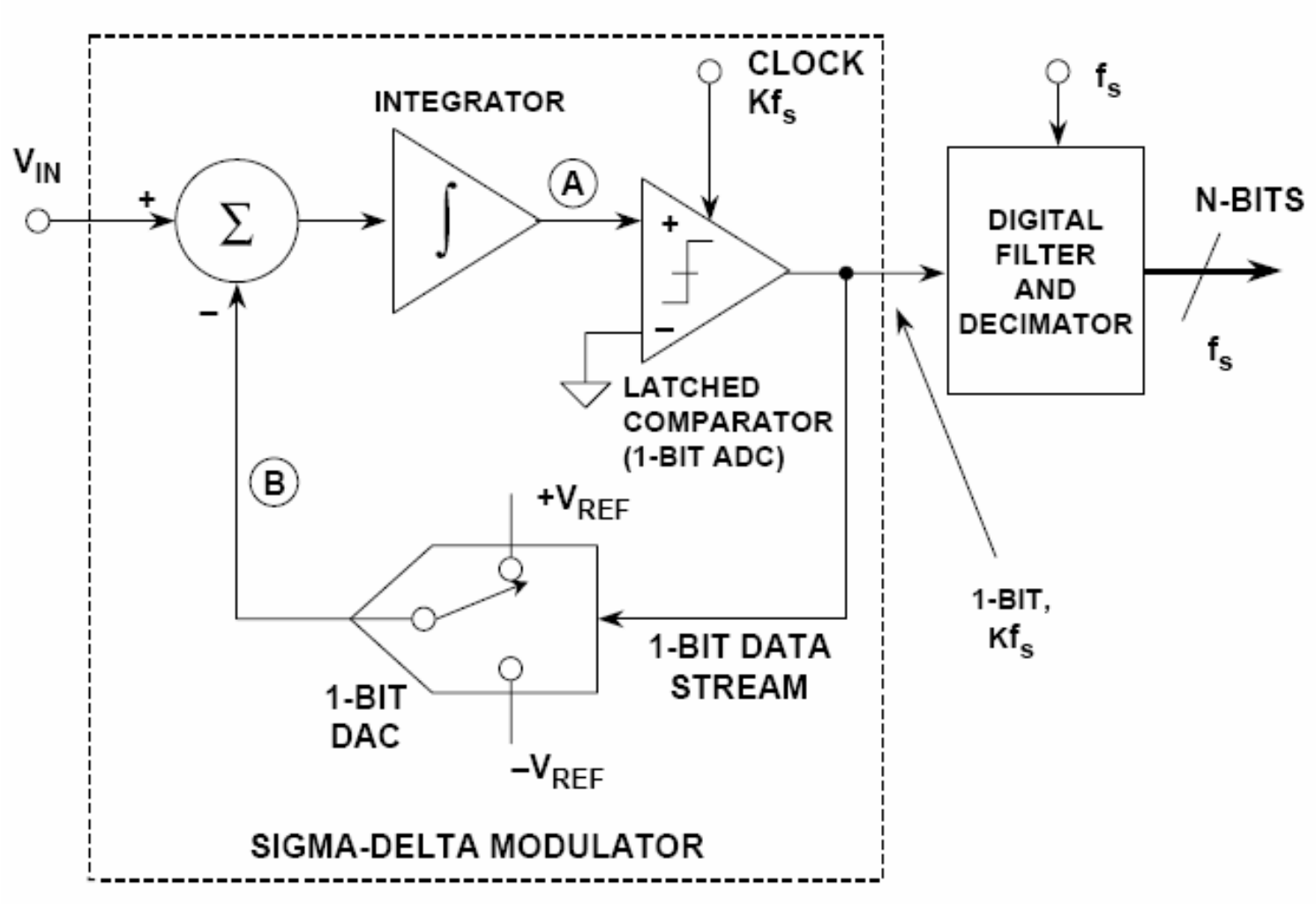
Sigma-Delta ADC

- Resolutions up to 24-bits
- Excellent differential linearity
- Internal digital filter (can be linear phase)
- Long throughput delay time (output latency)
- Difficult to multiplex inputs due to digital filter settling time

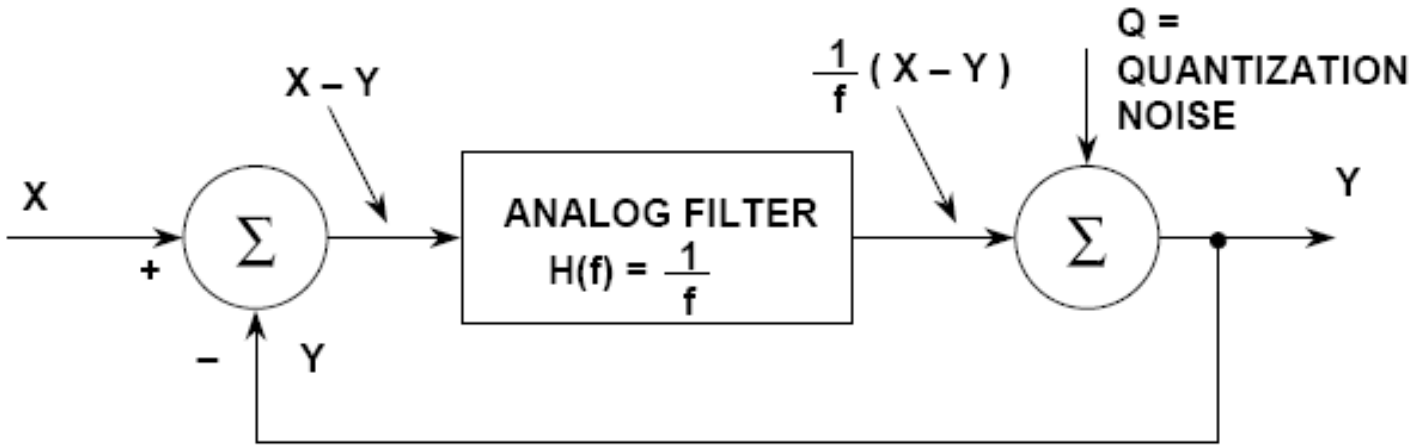
- Comparison of noise reduction techniques



- First-order Sigma-Delta ADC



- Linearized model of Sigma-Delta ADC



$$Y = \frac{1}{f}(X - Y) + Q$$

REARRANGING, SOLVING FOR Y:

$$Y = \frac{X}{f+1} + \frac{Q\,f}{f+1}$$

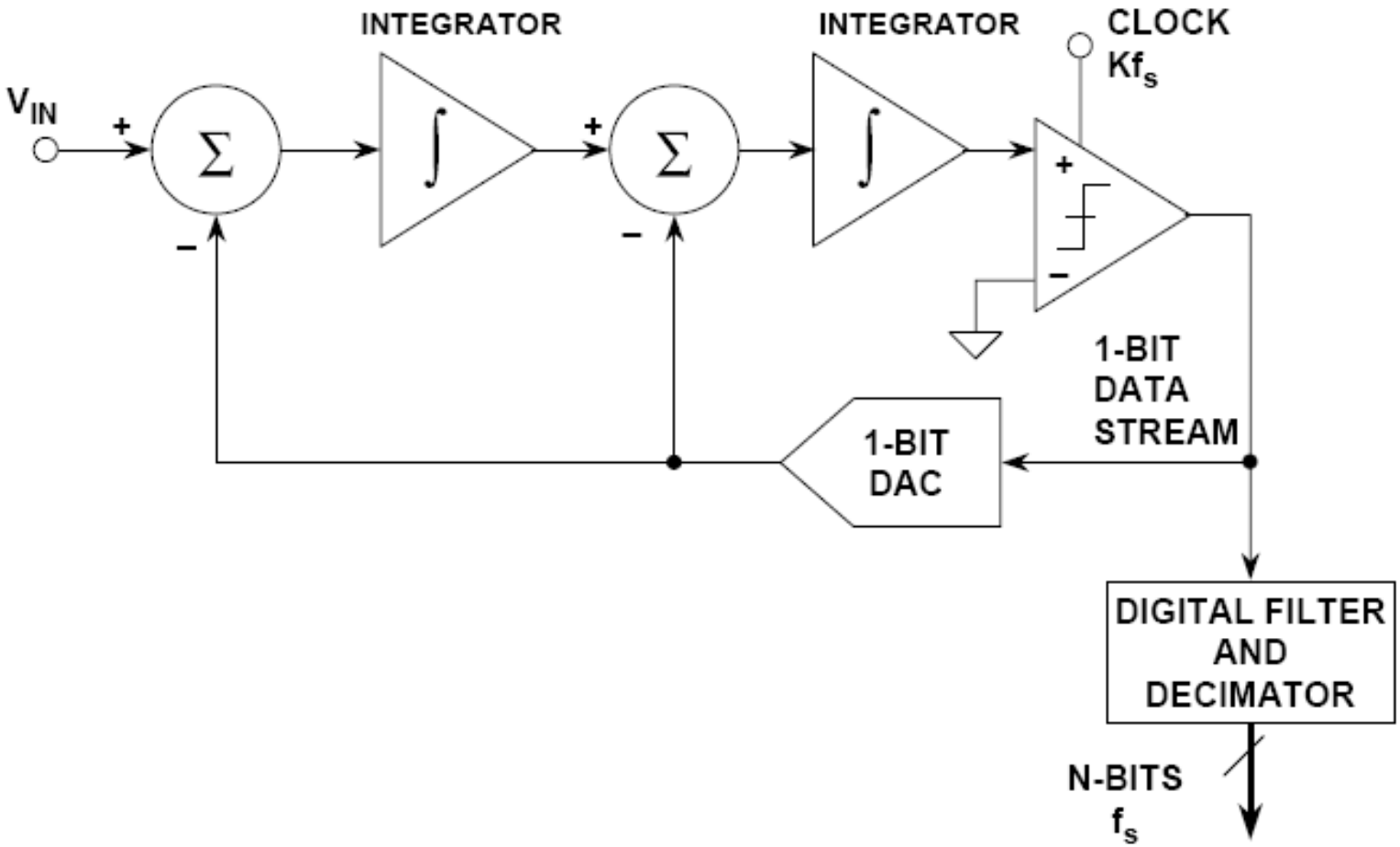
SIGNAL TERM NOISE TERM

- Frequency domain behaviour

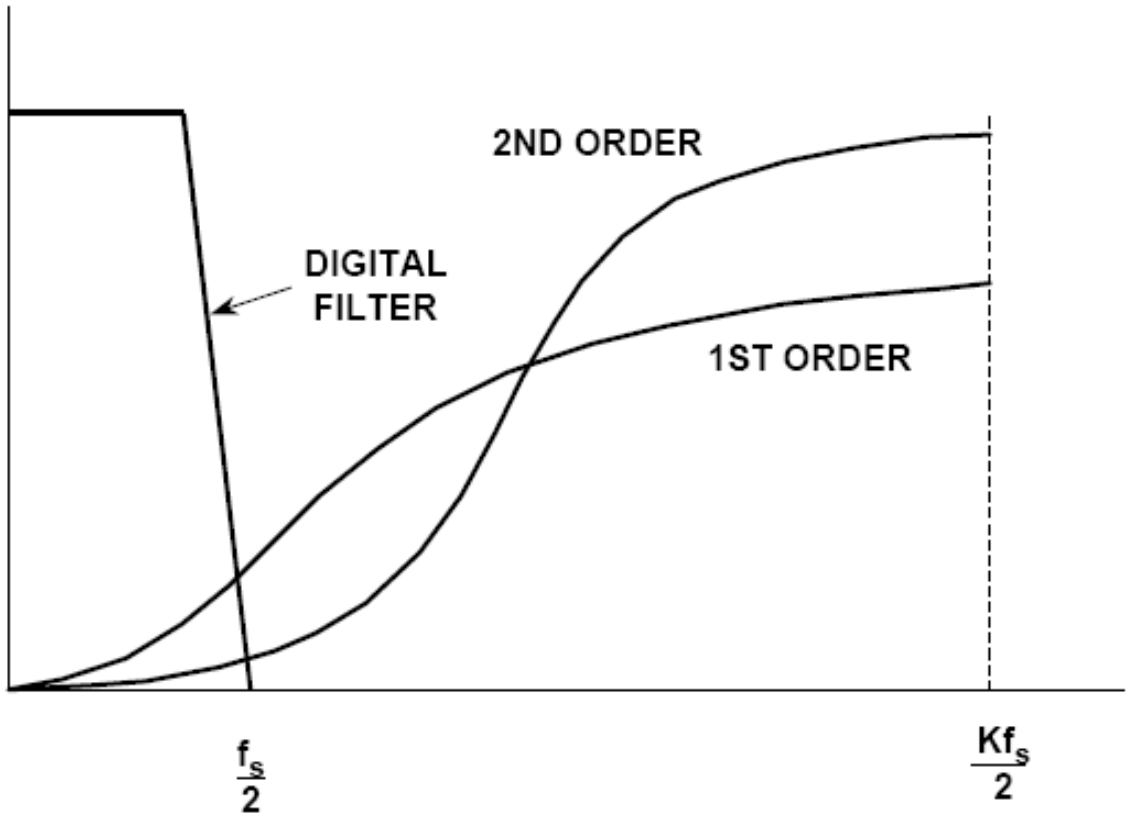
Y	X	Q
Low freq.	1	0
High freq.	0	1

- Using higher order filter: better supression
  longer settling
  stability issues

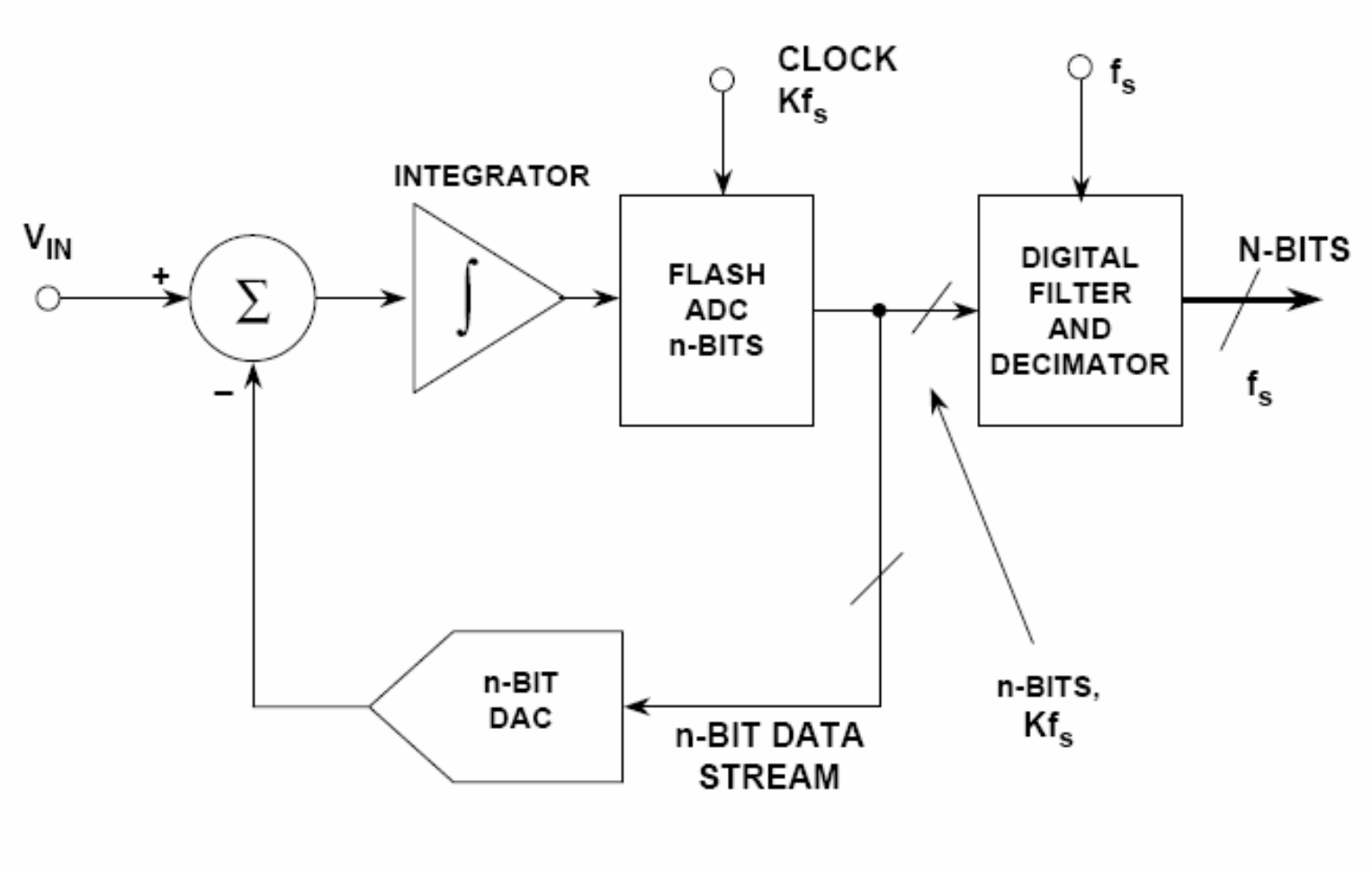
- Second-order Sigma-Delta ADC



- Noise reduction properties of Sigma-Delta ADCs



- Multi-bit Sigma-Delta ADCs



- Linearity problems
- Higher bit number can be achieved with the same oversampling ratio

- Application of Sigma-Delta ADCs
  - Mainly for audio (20-20kHz)
  - Typical bit number: 16-24 bits
  - Pros
    - Linear phase
    - Low cost (ideal for mass production)

– Cons:
  - Low sampling frequency
  - Cannot be multiplexed (one Sigma-Delta ADC per channel)

Characterization of distortions in signal analysis

- Harmonic distortion (dBc)
  - Harmonics fall at frequencies $|\pm K*f_s \pm n*f_a|$
    - f_s: sampling frequency
    - f_a: input signal frequency
    - n: order of harmonic
    - K is a natural number
  - Types: worst harmonic (largest value)

total harmonic distortion, THD= $\sqrt{\frac{\sum_N H_i^2}{A}}$

A: amplitude of input signal
H: amplitude of harmonic
N: number of harmonics

- Total harmonic distortion + noise (THD+N)

$$THD + N = \frac{\sqrt{\sum_{N} H_i^2 + \sum_{M} n_i^2}}{A}$$

  - n: noise+other disturbances excluding harmonics
  - M: defines the noise bandwidth

- Signal-to-noise ratio, SNR

$$SNR = \frac{A}{\sqrt{\sum_{M} n_i^2}}$$

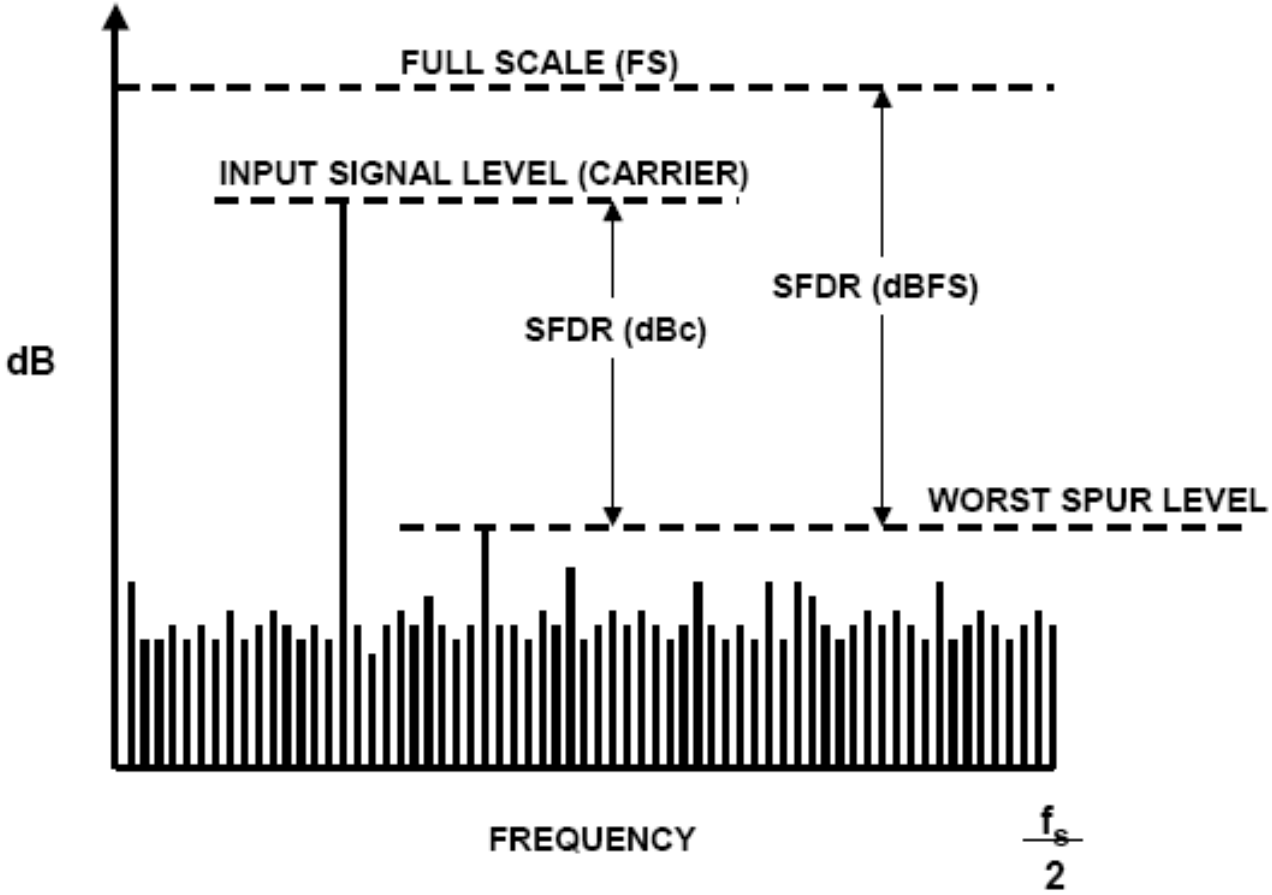
- Signal-to-noise and distortion ratio

$$SINAD=1/(THD+N)$$

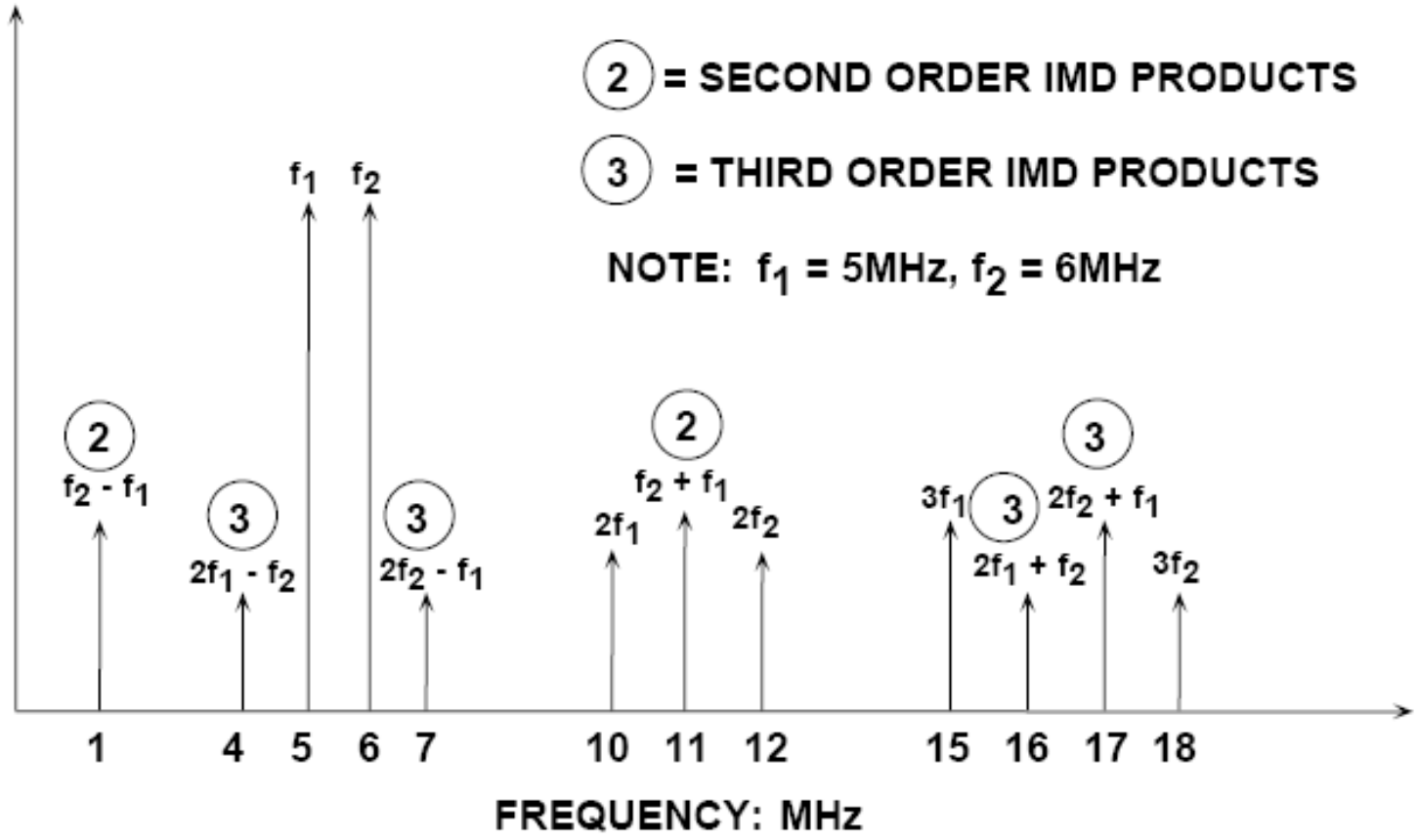
- Effective number of bits (in dB)

$$ENOB=(SINAD-1.76)/6.02$$

- Spurious-free dinamic range

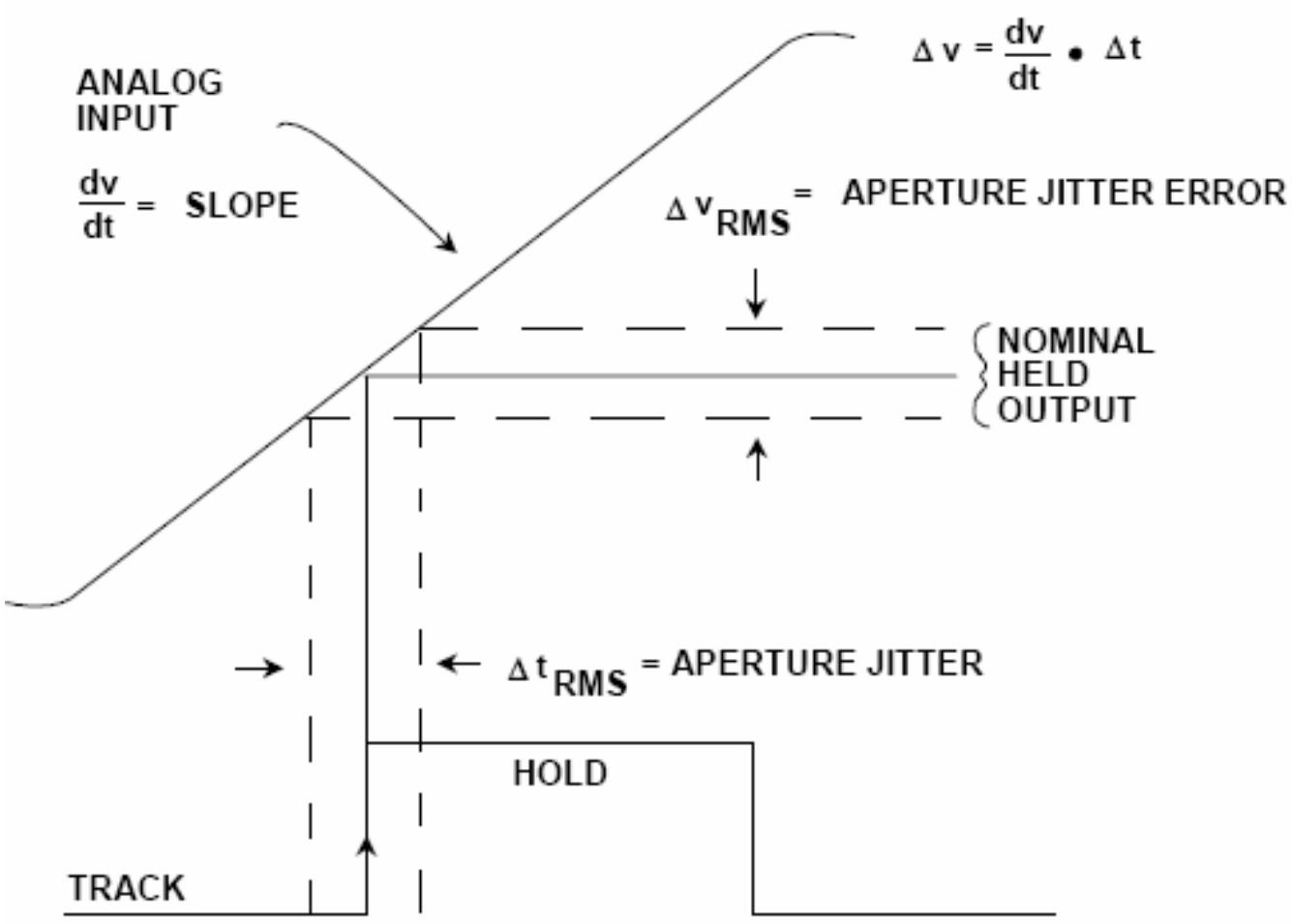


- Intermodulation distortion



Jitter

- Uncertainity of sampling time instant



References

- Analog Devices: Basic Linear Design
- Analog Devices: ADCs for DSP Application