Field Programmable Gate Array (FPGA)

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FPGA in general

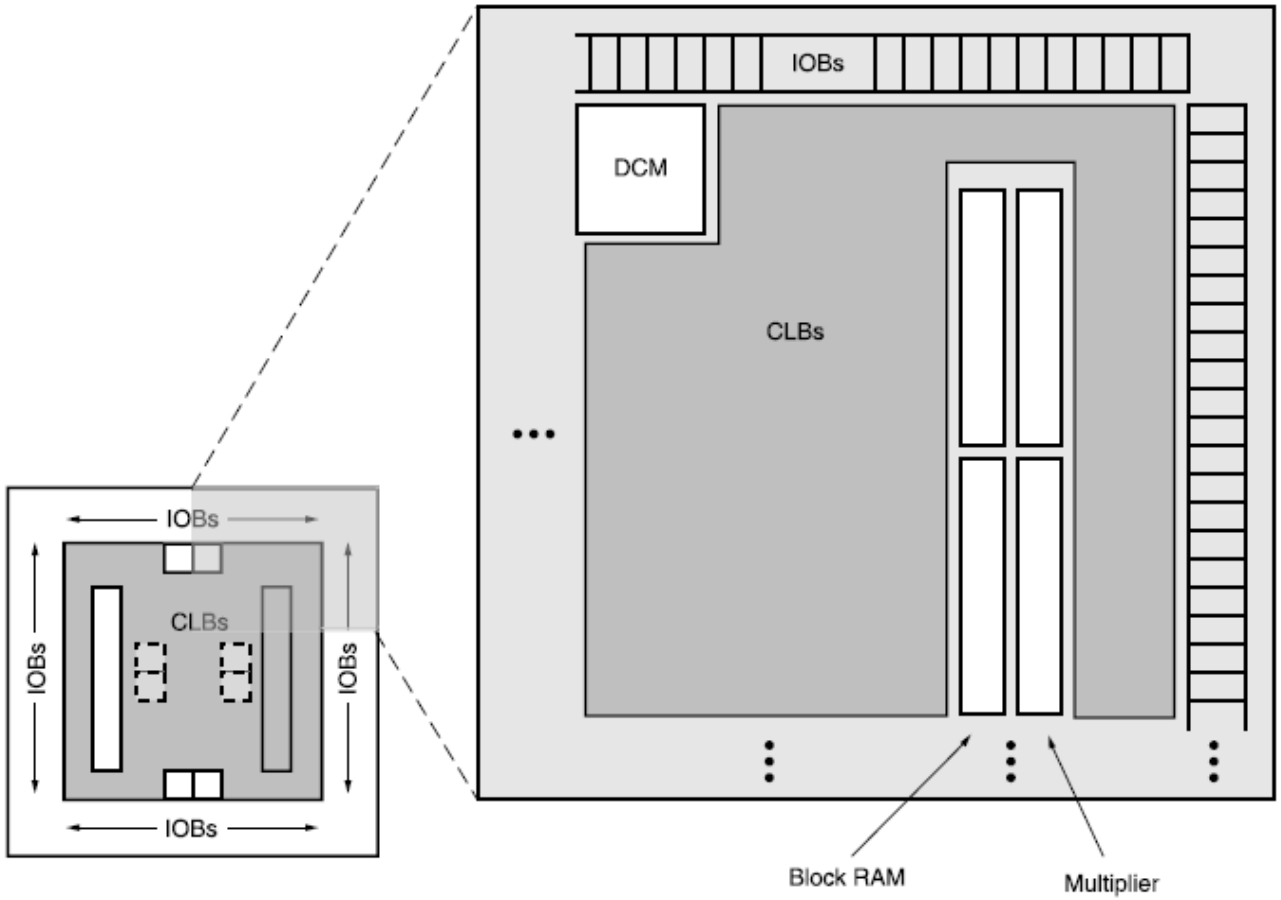
- Reprogrammable Si chip
- Invented in 1985 by Ross Freeman (Xilinx inc.)
- Combines the advantages of ASIC and uC-based systems
- HW-timed -> fast operation and realiable
- Cheap even if the volume is low (in contrast to ASIC)

FPGA vs. uC-based systems

- Similar flexibility
- FPGA: execution speed is not limited by the number of processing cores
  - Parallel in nature
  - No competition for system resources
  - Processing tasks are assigned to dedicated chip sections
    - Autonomous opration of functions
    - Performance is not affected by multiple tasks

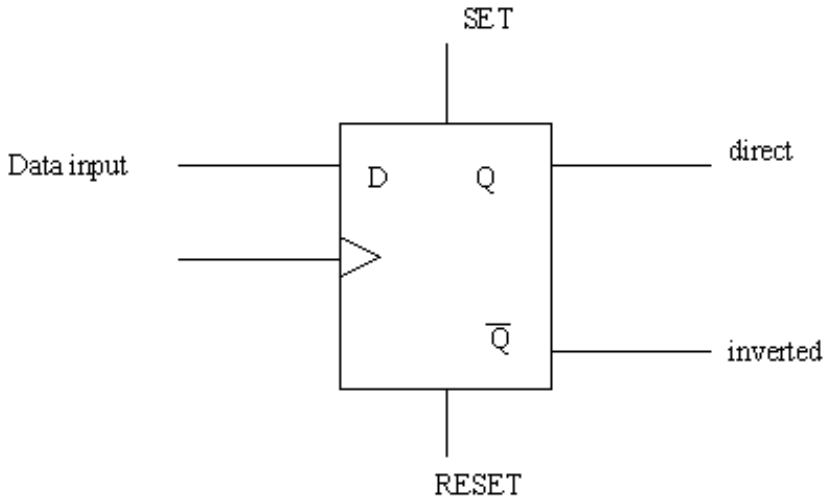
- How is it achieved?
  - Application logic is implemented in HW not by executing on top of OS in SW

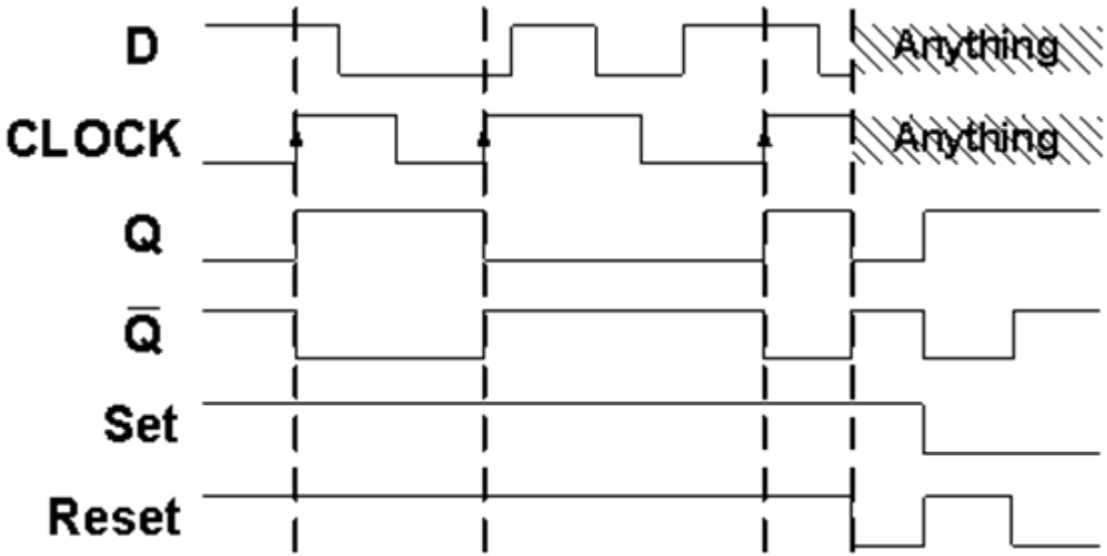
Building blocks of FPGA



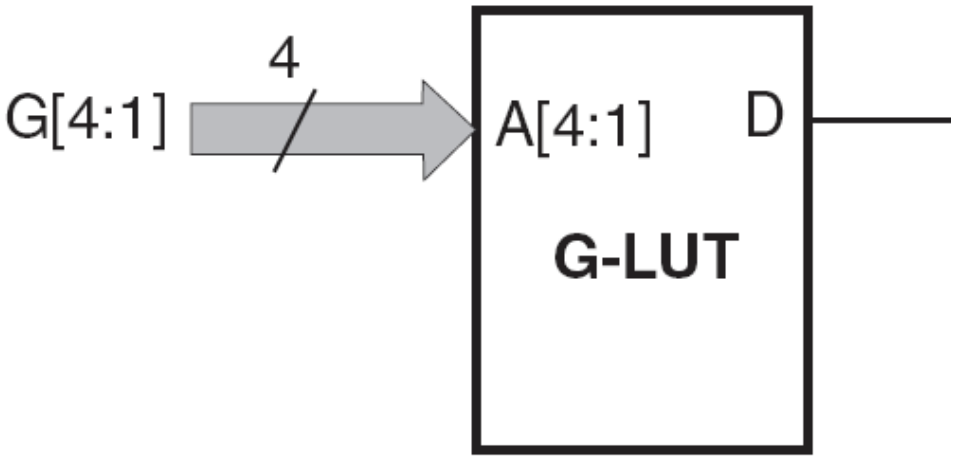
Xilinx Spartan 3E family architecture

- FPGA is built up of a finite number of predefined resources
  - Configurable logic block (CLB) (slices, logic cell)
    - Basic logic unit of FPGA
    - Made up of two basic components
      - Flip-flops (FF)
      - Look-up-tables (LUT)
  - FF: on every CLK edge FF latches 1 or 0 on its input and hold that value constant until next CLK edge-> binary shit register


SET
Data input
D
Q
direct
$\overline{Q}$
inverted
RESET


D
CLOCK
Q
$\overline{Q}$
Set
Reset
Anything
Anything

– LUT:
  - Provides mucs of the logic of CLB
  - Small amount of RAMs
  - Logic is implemented as truth tables within LUT memory
    – Truth table: predefined list of outputs for every combination of inputs



- Example for implementing logic function: AND operation

INPUT		OUTPUT
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

- Input/output blocks (IOBs)
  - Control the data flow between the I/O pins and the internla logic
- Digital CLK manager (DCM)
  - Distributing, multiplying, dividing CLK signal
  - Different CLK rate is possible for different FPGA sections
- Fixed-function logic block
  - Prebuilt processing block to save FPGA resources
  - Example: multiplier blocks
    - Dedicated multiplier associated with RAM

- Block RAM (BRAM)
  - Configurable, user-defind RAM
  - 16-36 kbyte
  - Used for
    - Data storage
    - Passing data between logic blocks running at different CLK rates

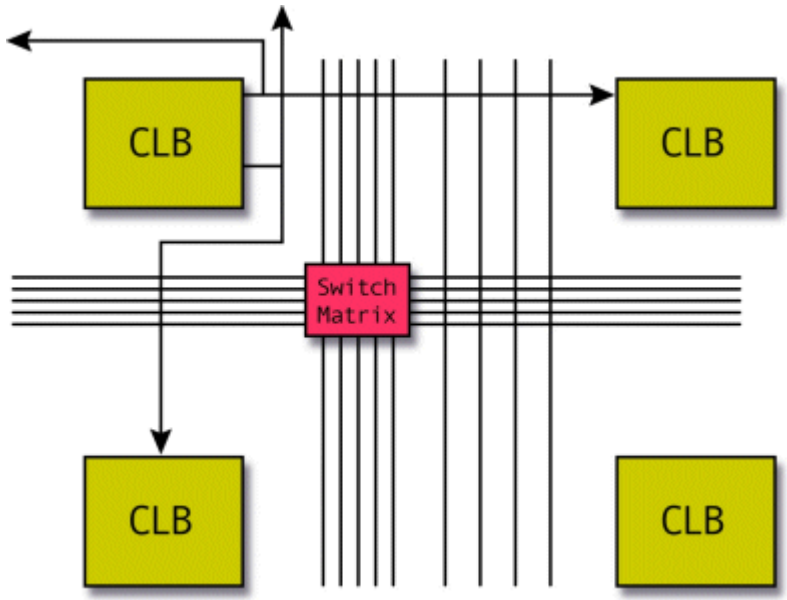
FPGA-based systems

- No driver system or code-based system (that uP and OS have)
- Communications to peripherals is difficult
- Hybrid architecture: uP is paired with FPGA and connected to I/O
- Implementation
  - System components and their interconnections (wiring) has to be defined by design SW

- In the past only low-level design solution existed
- Now hig-level synthesis (HLS) design tools available
  - HW description languages (HDL)
    - Verilog, VHDL -> text based
- Even higher level design languages
  - Graphical-based (G-code) languages

(Note: coding in HDL in out of the scope of this subject)

- The code is compiled and a bit file is generated to be downloaded on the FPGA
  - It defines the circuit itself (blocks and interconnections)



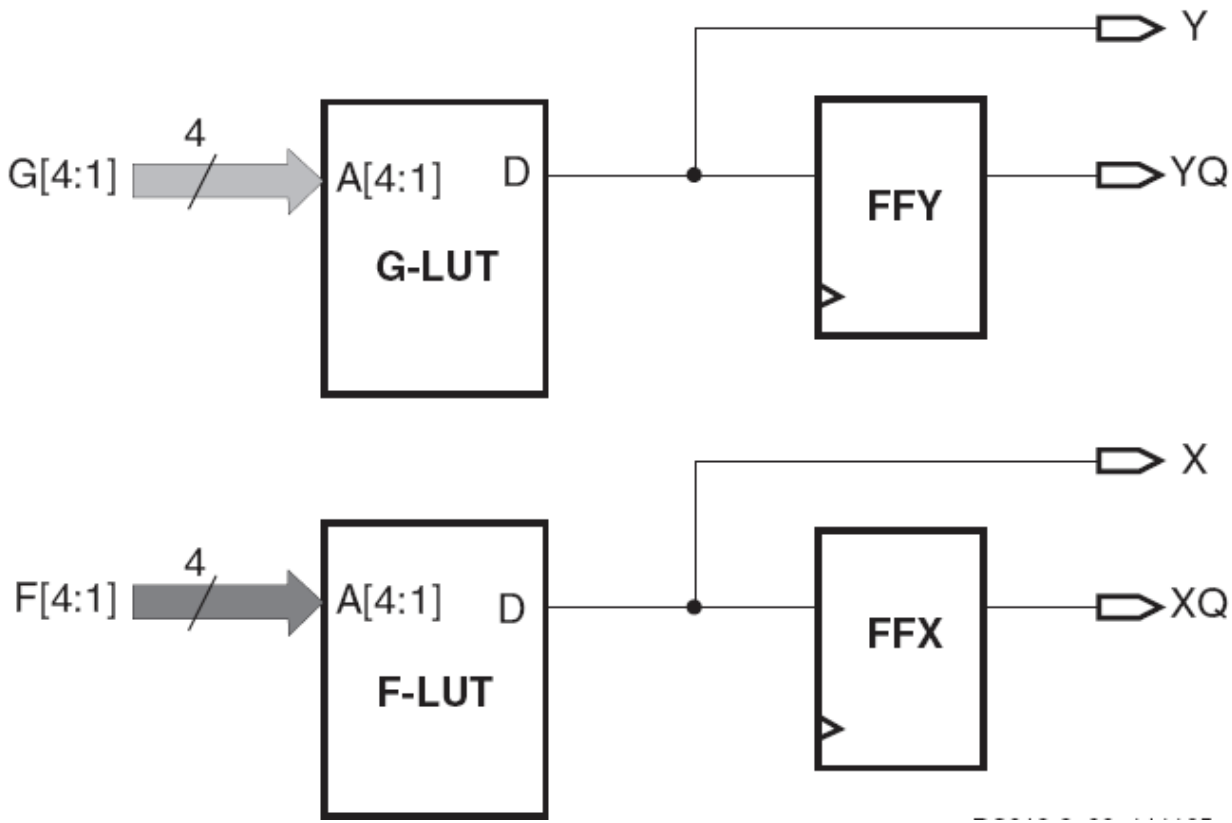
Reconfigurable interconnections

- Fusible link
  - Not reversable
  - Applying a high-voltage pulse disconnects the wires
- Antifuse link
  - Not reversable
  - Applying a high-voltage pulse connects the wires

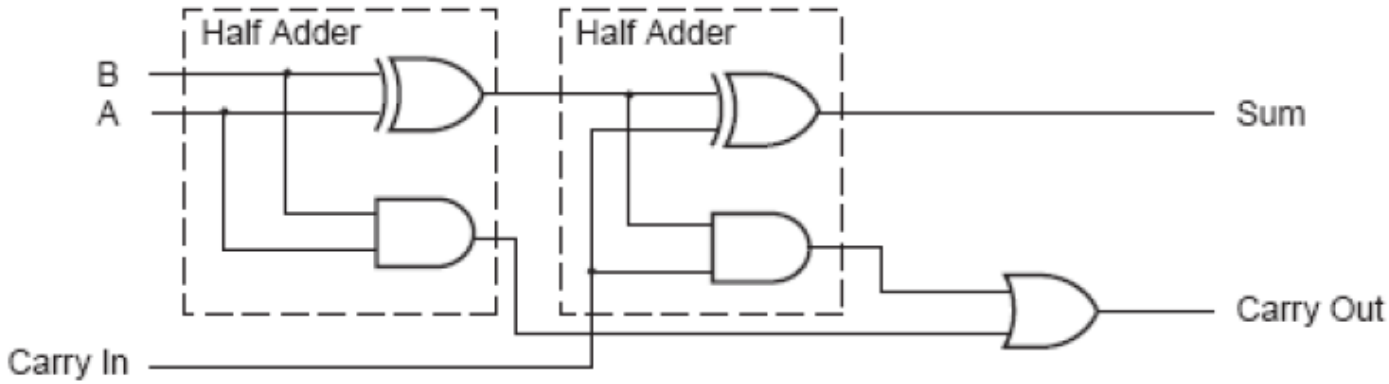
- Flash transistor
  - Switching the transistor to on/off state controls the connection of wires
  - Reversable
  - Non-volatile (if power off, the state is preserved)
- SRAM-based
  - Most widely used
  - Reversable
  - Volatile (reprogramming is needed at every startup)

Resources of CLB

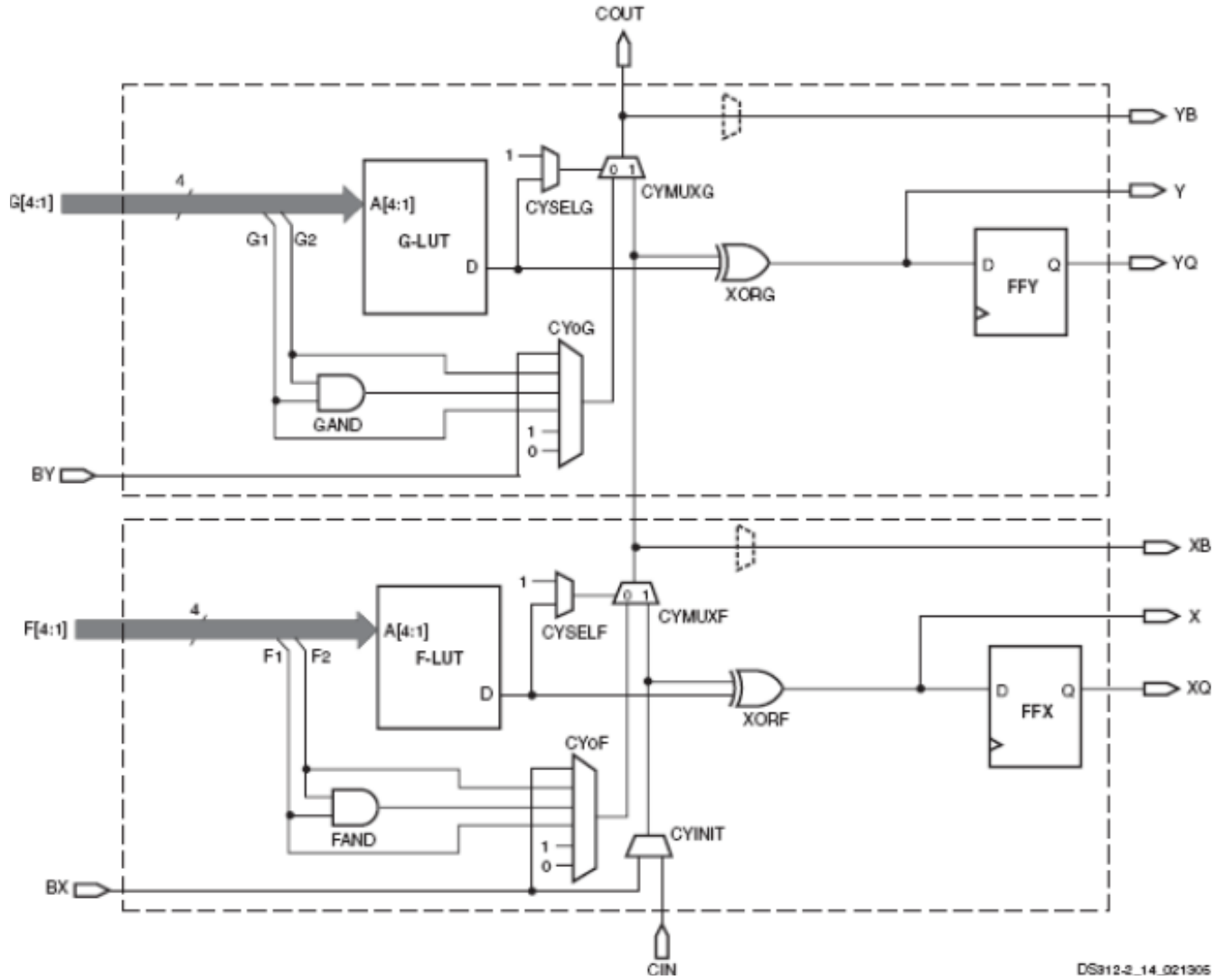
- Resource unit = logic cell = 1LUT+1FF
- In a slice:



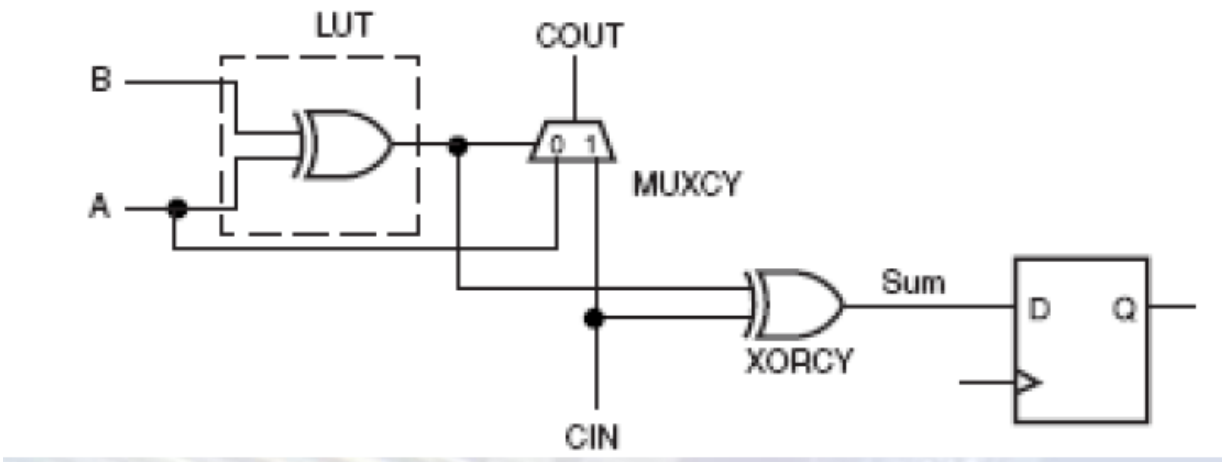
- Logic functions of many variables requires to many levels of logic cells -> slow
- Arithmetic operations requires carry-bit
  - Fast carry generation is a must
  - Example: full adder



- Full adder implemented on FPGA:



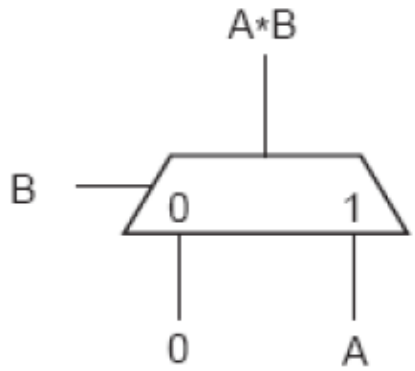
Fast carry generation



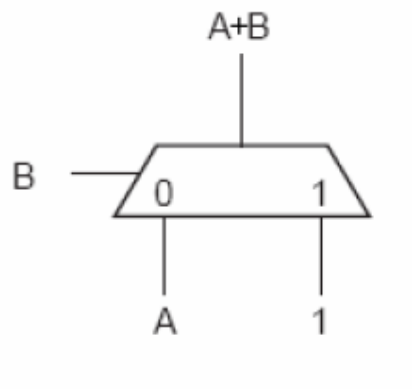
- Sum=A xor B xor C
- Carry: propagation/generation
- Cout=A*B+A*Cin+B*Cin

  (A xor B)?(Cin:A) selects either Cin or A

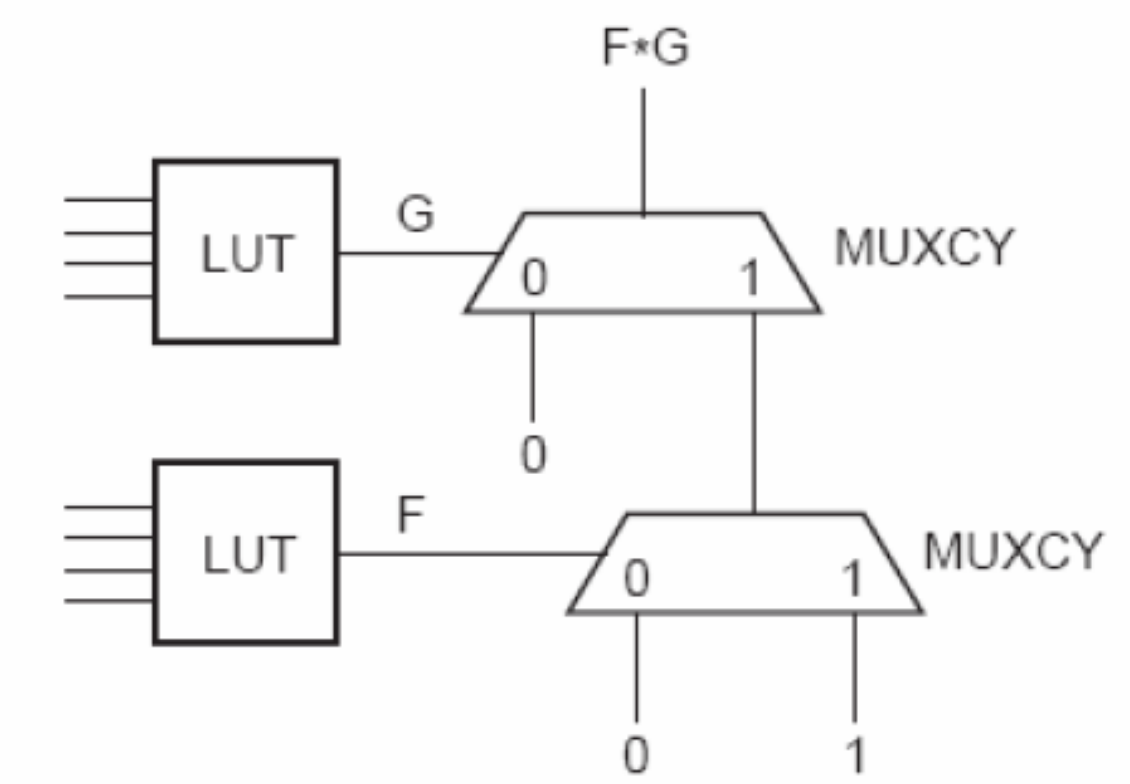
- Application of multiplexer (MUX) for logic
  - MUX-based AND:



  - MUX-based OR:

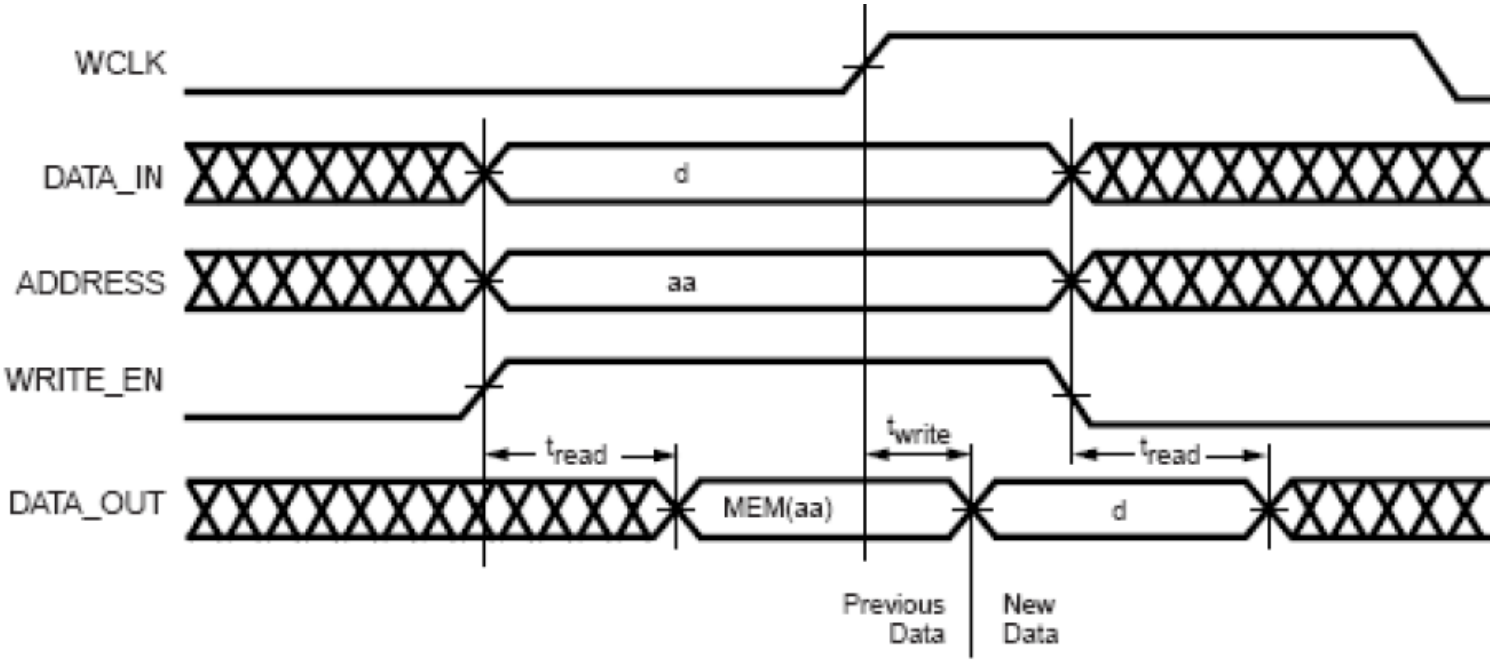


- Combining LUT4s using MUX
  - „wider” logical functions

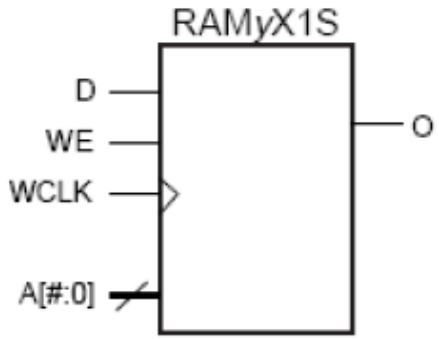


LUT RAM

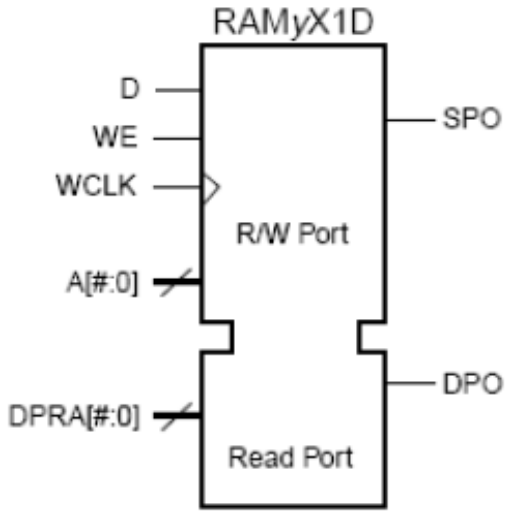
- Writing is synchronous
  - CLK edge -> writing starts
- Reading async -> independent of CLK



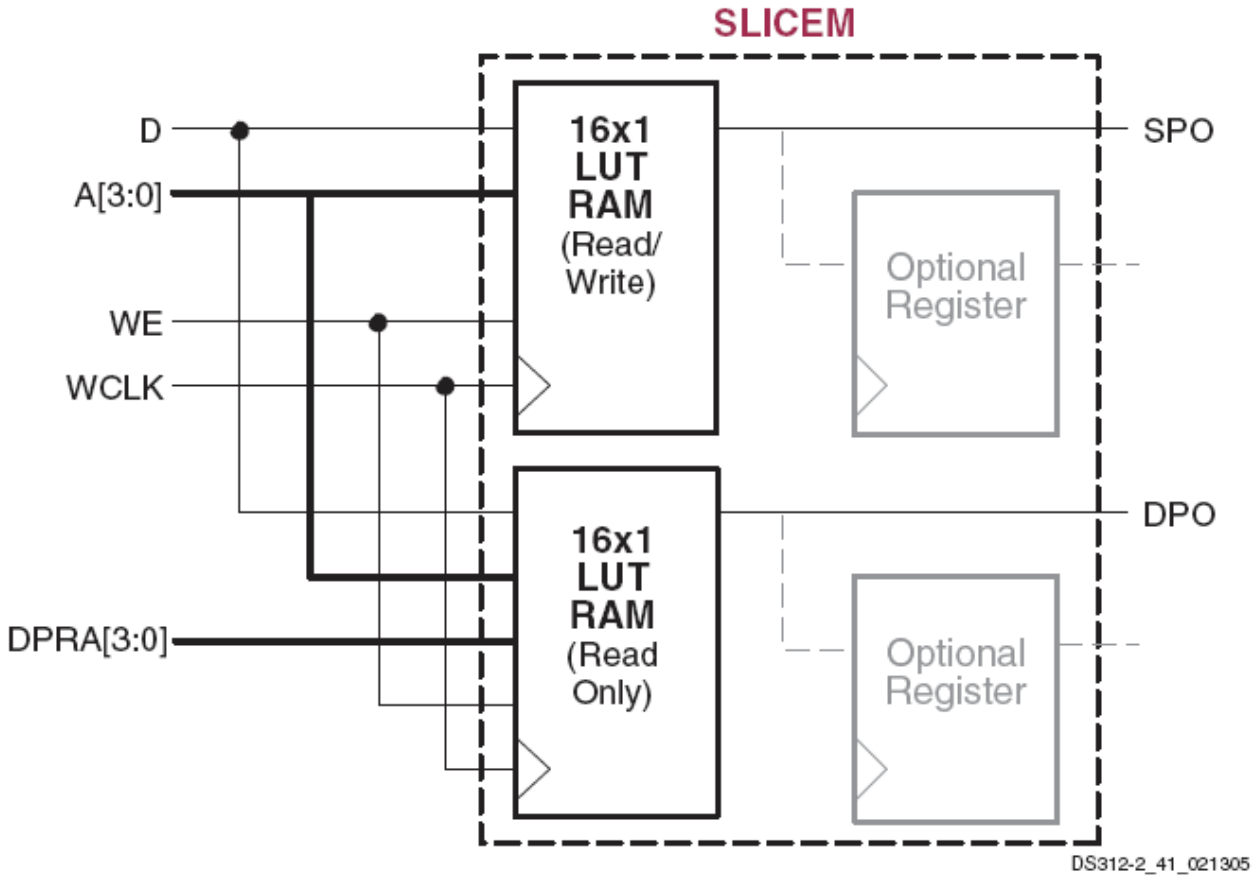
- Distributed RAM
  - Single port RAM: read or write access allowed one at a time



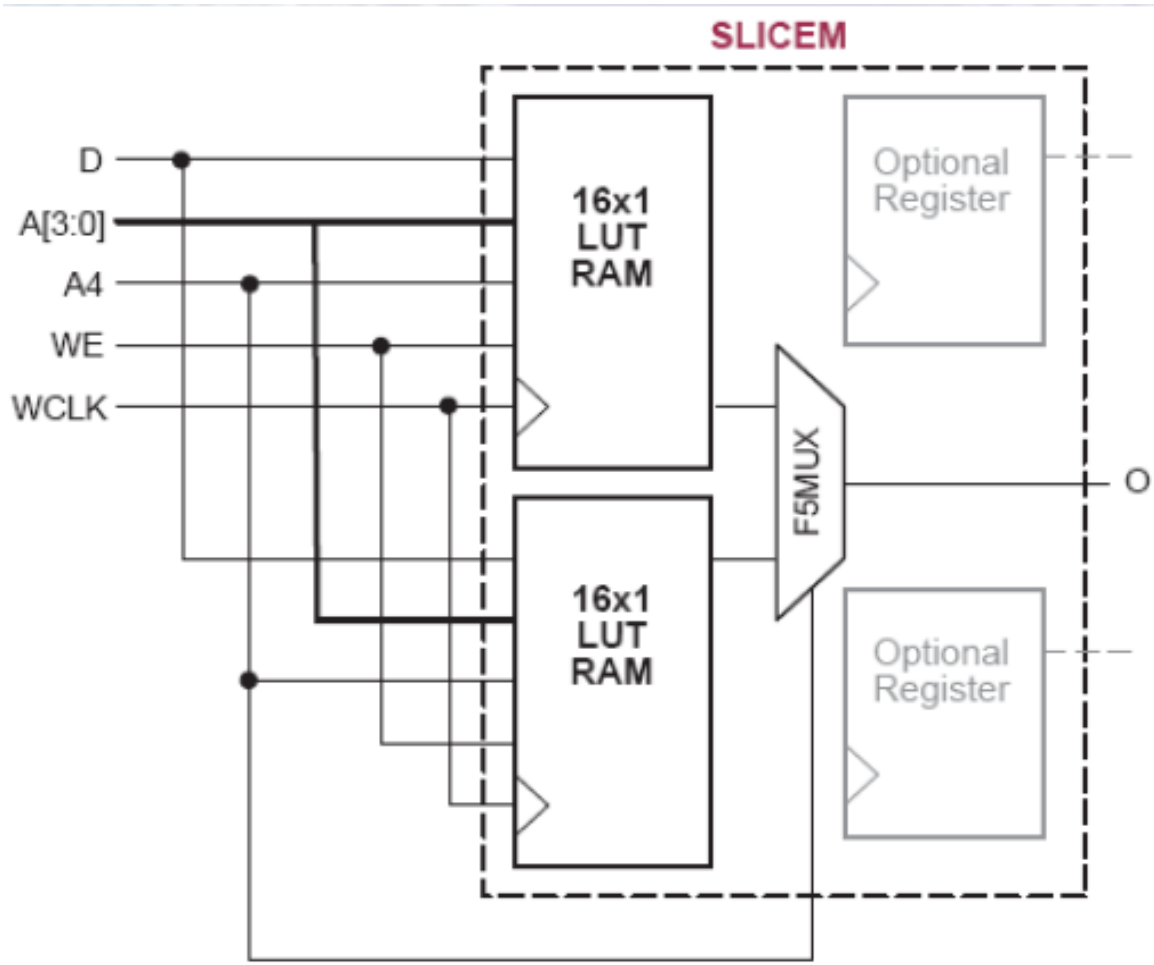
  - Dual port RAM: read or write possible at the (nearly) same time



- Realization: in one slice
  - one RAM16x1D or …



- …one RAM32x1S



- Size of RAM (data width) can be increased
  - RAM32x8S -> 8 slices are used

Slice M:

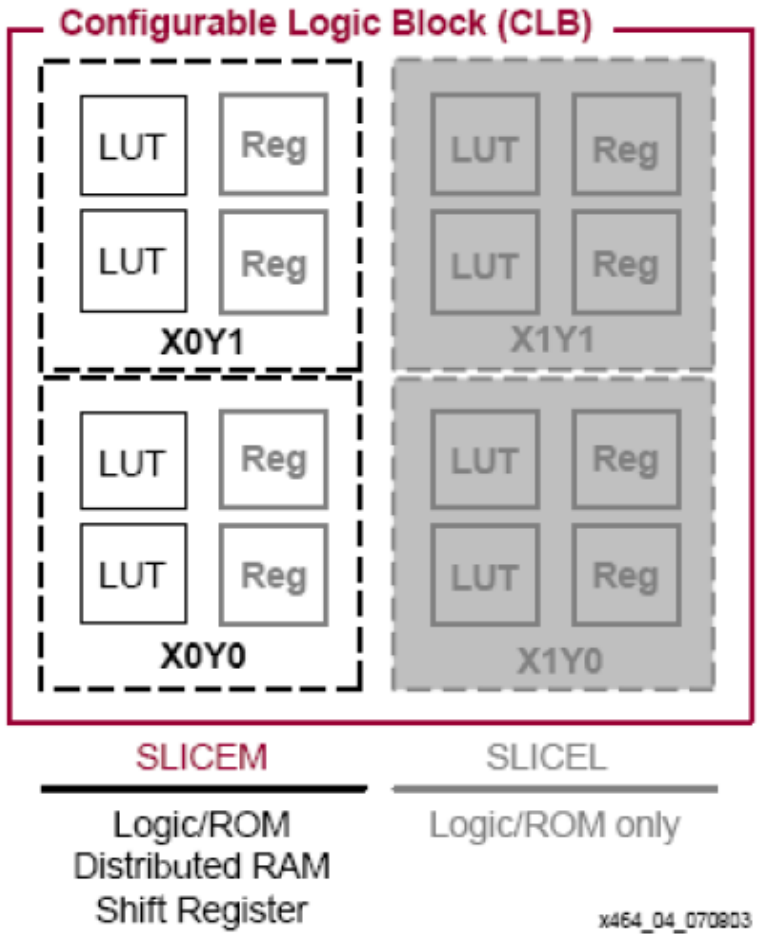
Logic/ROM

Distributed RAM

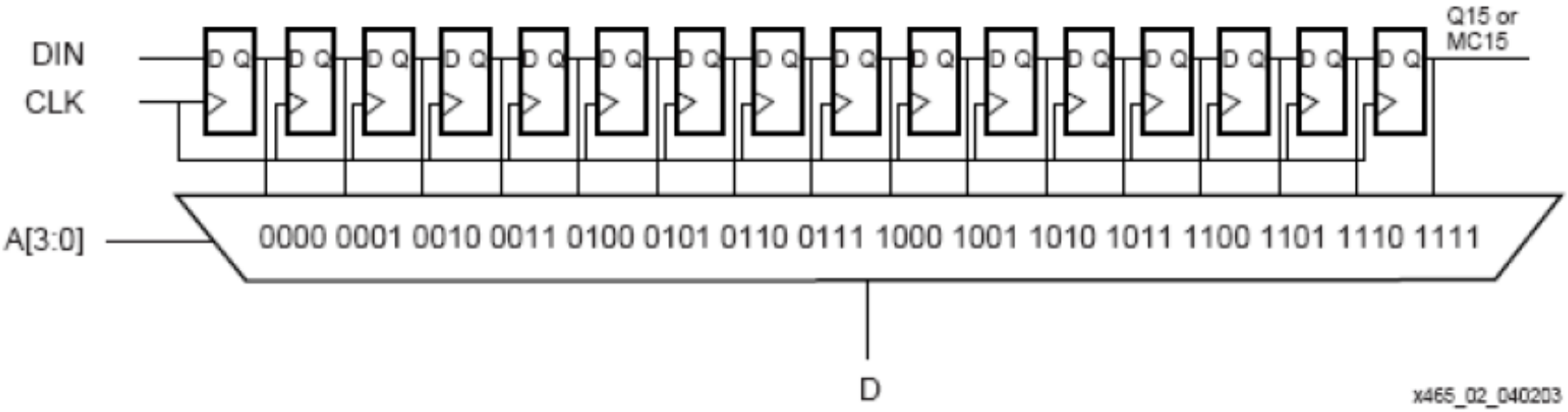
Shift register

Slice L:

Logic/ROM only

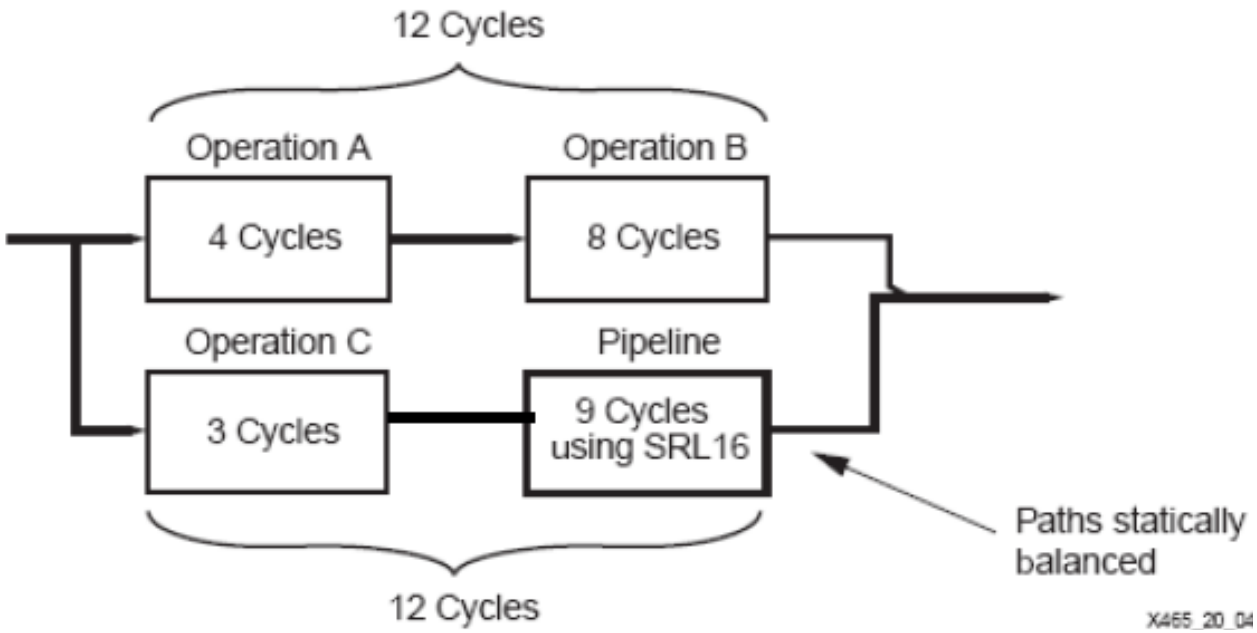


LUT shift register (SRL16)



- Felxible applications
- Serial delay of variable length (1-16)
- Can be cascaded to neighbouring CLBs

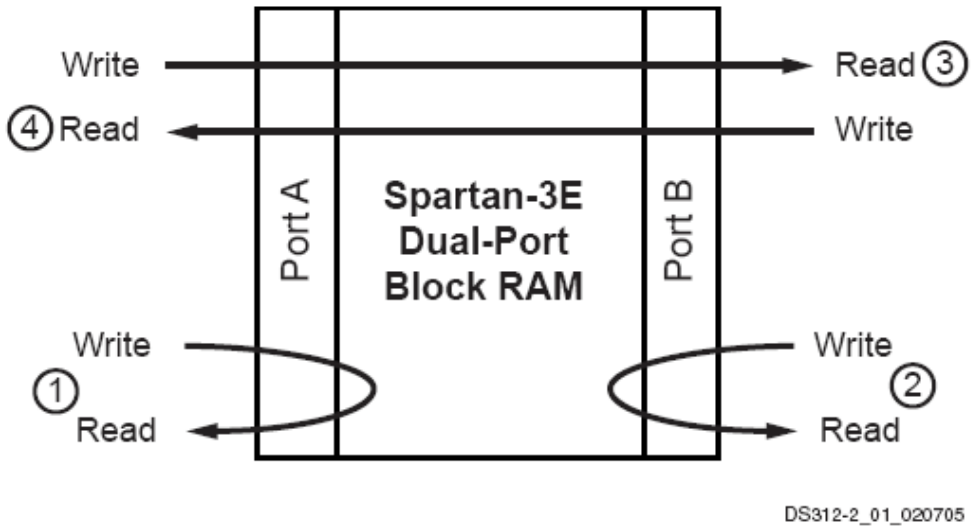
- Typical application of LUT SRL
  - Balancing delays caused by pipe-line
    - Data width determines the number of LUTs



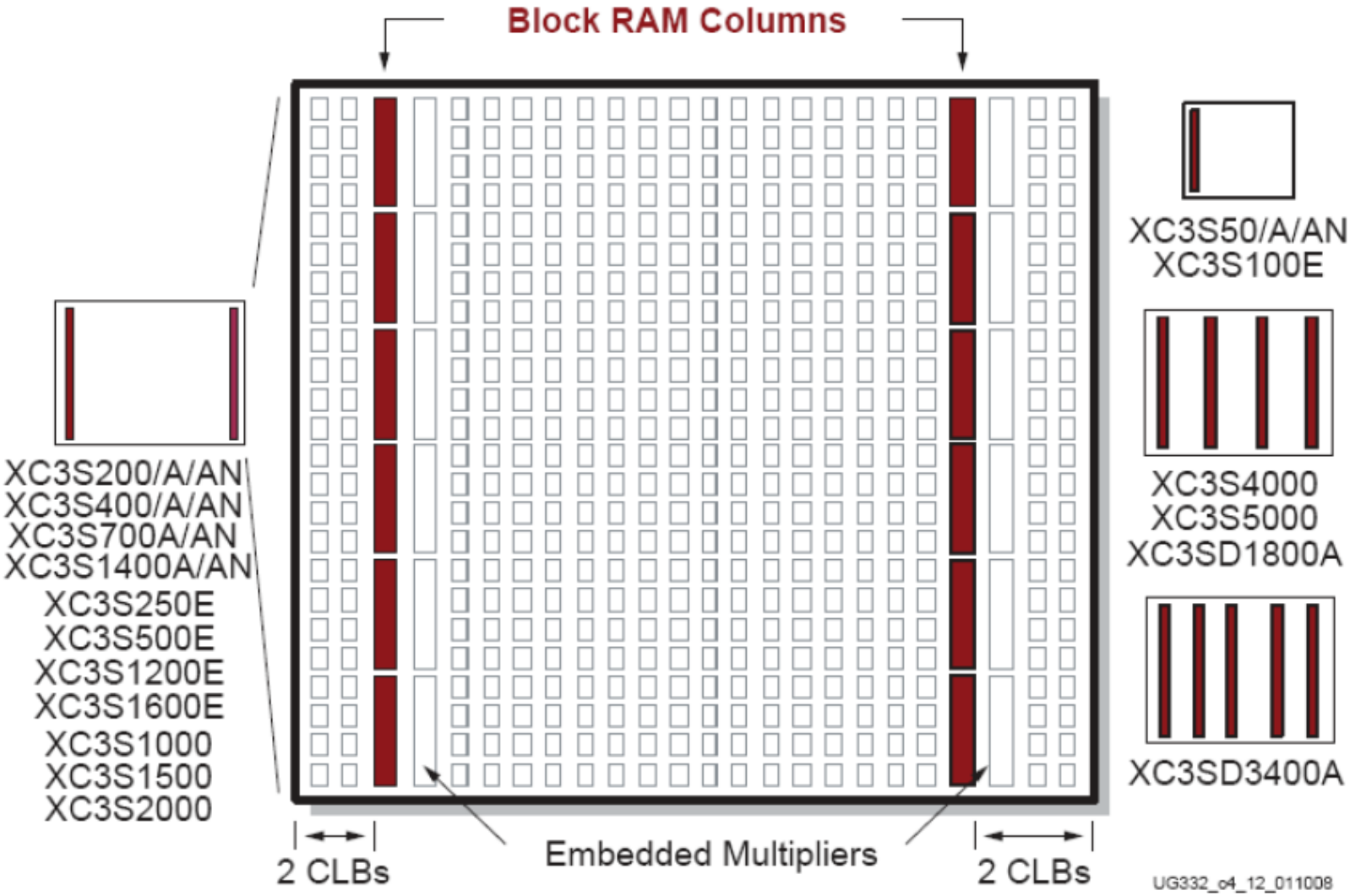
- Small FIFO
  - Data in SRL
  - Auxiliary logic
  - Address counter
  - Status indicator
- Random number generator
- Code generator
- Counter

BRAM

- 2-4 kbyte dual port synchronous RAM
- 4-36 pieces
- Data width can be changed dynamically
- R/W options:



- BRAM on the FPGA

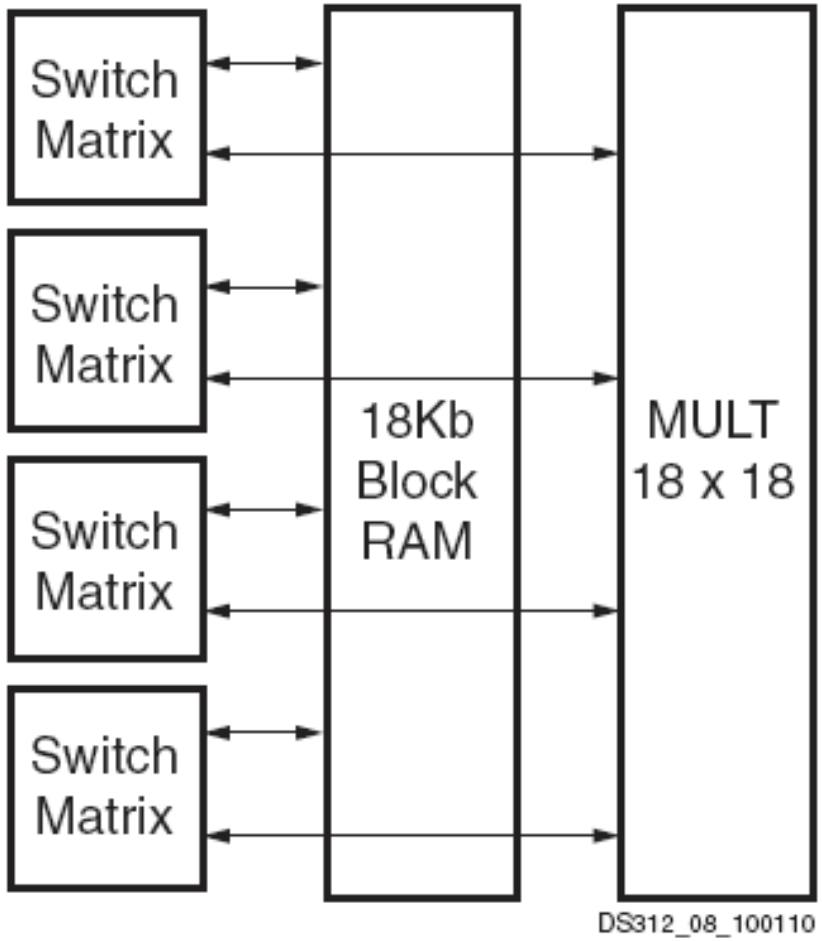


- BRAM is used for
  - data exchange between different CLK rate sections
  - as a logic circuit similar to a big LUT
  - storing tables (sin(); cos(); etc.)

Multiplier

- Full parallel 18x18-bit multiplier
- Matched to BRAM 18-bit configuration
- FIR filtering supported
- 2’s complement -> signed operations
- 36-bit result
- Can be extended to 35x35-bit

- Block diagram of interconnects with multiplier



I/O blocks

- Connection between FPGA and outside world
- Several I/O standard supported
  - Single ended: LVCMOS 1.2; 1.5; 1.8; 2.5;3.3V
  - Differential:
    - LVDS – low-voltage differential signalling
    - SSTL – stub series terminated logic
    - TMDS – transition minimized differential signaling

- Three state driver
- Registers
- Programmable delays (IODELAY)
- Transceiver

Clock source management

- Very important part of the design
- Synchronous operation is required
  - One CLK in one block/module
    - Slower scheduling implemented by CLK driven enable input
  - For the whole design different CLKs possible
    - Careful design between blocks using different CLKs

- Global CLK network
  - Die are divided into 4
    - Each ¼ has 8-8 global CLK network
      - Can be used independently vs. Globalized
        - » Matter of energy consumption
    - Driving only by global CLK buffer (BUFG)
    - Sources of CLK
      - External
      - CLK handle modul output
      - Any internal signal

- Features
  - Only minimal delay of CLK on the whole FPGA area
  - Cannot be used as logic signal
  - CLKs can be changed by MUXs
  - Can be used for
    - Synchronization
    - Frequency divider
    - 2x frequency multiplier
    - Phase shifter/splitter
    - PLL frequency synthesizer

References

- Xilinx Spartan-3E FPGA Family Data Sheet
- Xilinx online resources