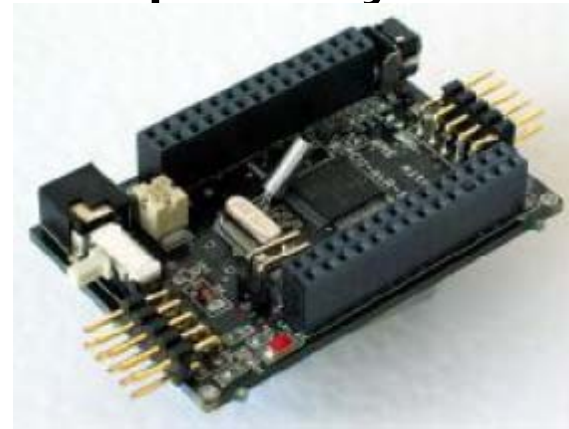


Microcontroller HW and SW platforms

Lecturer: Krébesz, Tamás

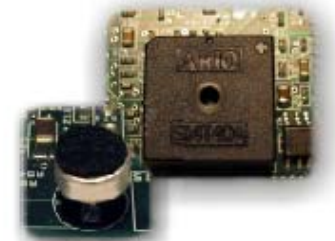
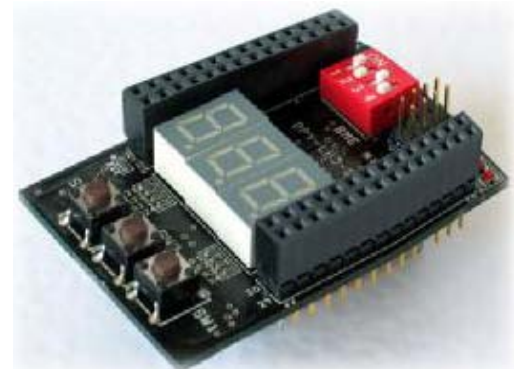
MITMÓT

- Modular mote system developed by BME-MIT
 - Processor modules
 - 32-bit ARM core
 - 8-bit ATMEL core
 - Communication modules
 - Radio 1: 433-866 MHz
 - Radio 2: 2 GHz, ZigBee
 - Ethernet
 - Power line



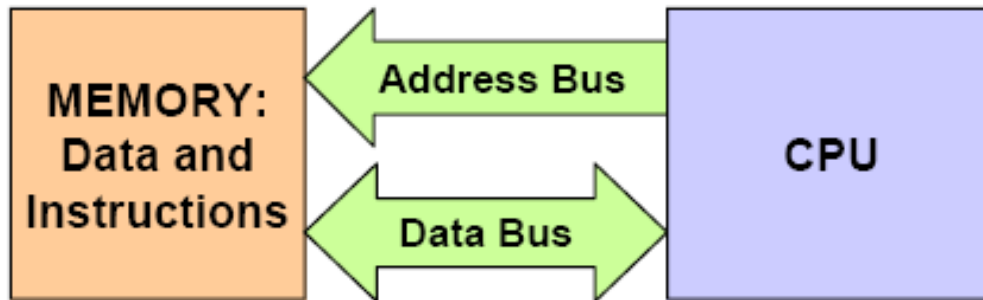
– Sensor, actuator modules

- Basic I/O module
 - LED, 3-digit display
 - Pushbuttons, switches
 - I2C thermometer
- Acoustic module
 - Analog in/out
 - Mic, speaker
- DC motor driver module
 - 2 DC motor drivers
 - 2 rotation sensors



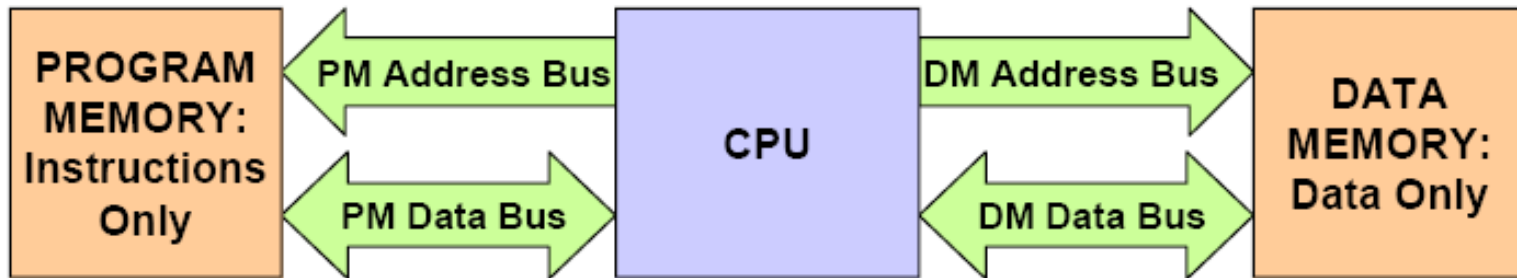
uC architectures

- von Neumann



- Shared bus system and memory for program and data -> limited system performance
- Self-modifying code is possible
- General purpose computers, traditional uC

- Harvard



- Separate memories for data and program -> different bus size is possible
- Faster data fetch and so processing
- Program cannot be self modifying

- Main general features of 8-bit uCs
 - Harvard architecture
 - 8-bit data bus
 - Address bus can be wider 14-16-bit (PIC16: 14-bit)
 - RISC – reduces instruction set computer
 - Generally 1 instruction / 1 clock pulse
 - » fetch+operation+store
 - Speed: 8-20 MIPS – million instruction per second
 - Static operation
 - Clock rate reduced -> power consumption reduced
 - Clock can be changed on needs -> can be 0, but <20MHz
 - Memory: RAM n*k, Flash 128k, EEPROM

- Power-on-reset: keeps resetting until power level stabilized after turning on the device
- Timer: 8-16-bit
- ADC: 8-10-12-bit (SAR ADC)
- PWM (pulse width modulation) output:
 - Using one of the timers
 - Usually can be used as DAC
- GPIO: general purpose I/O
- UART/USART: universal asynchronous/synchronous receiver transmitter

- SPI: serial peripheral interface
- I2C: inter-integrated circuits
- CAN: controller area network
- LIN: local interconnect network
- Interrupt: priorities, shared
- Reset
- Watchdog: detect & recover from malfunction
- Ports: TTL or Schmitt-trigger input

Development platform

- AVR Studio
 - Integrated development environment (IDE) for writing and debugging AVR applications
 - Free to download from ATMEL webpage
 - AVR Studio 4.19. Build 730
 - Assembler: SW that translates assembly code into machine code
 - Compiler: code written in higher level language translated into assembly or machine code directly

- Make file: a type of script that pass parameters for the compiler, loader, contains information of the compiling process and source files
- JTAG ICE
 - HW (converter chip)+SW for on-chip debugging
 - Happy JTAG: freeware SW to interface between AVR Studio and converter chip

- WinAVR
 - Tool chain under AVR Studio
 - Includes compiler for C/C++ (by GNU-GCC)
- MITMÓT system SW level considerations
 - CPU independent bus system
 - API – application programming interface
 - HW dependent: open HW specification
 - HW independent: application layer can be handled independently from the HW on a general SW platform
 - Advantage of the layered structure

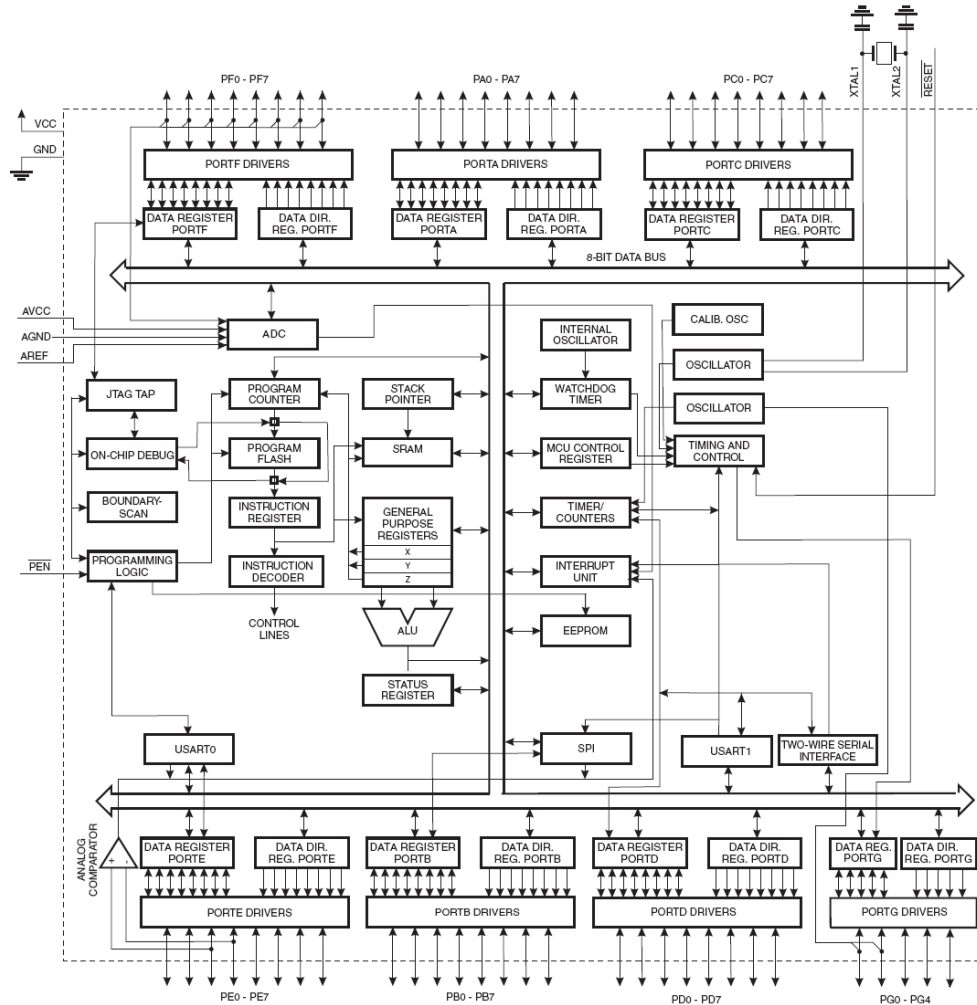
ATMEL AT Mega 128 uC

- Main features
 - Harvard architecture
 - 8-bit data bus
 - RISC, 133 instructions
 - Static operation
 - Max. 16 MHz crystal oscillator: 16 MIPS
 - On-chip HW multiplier

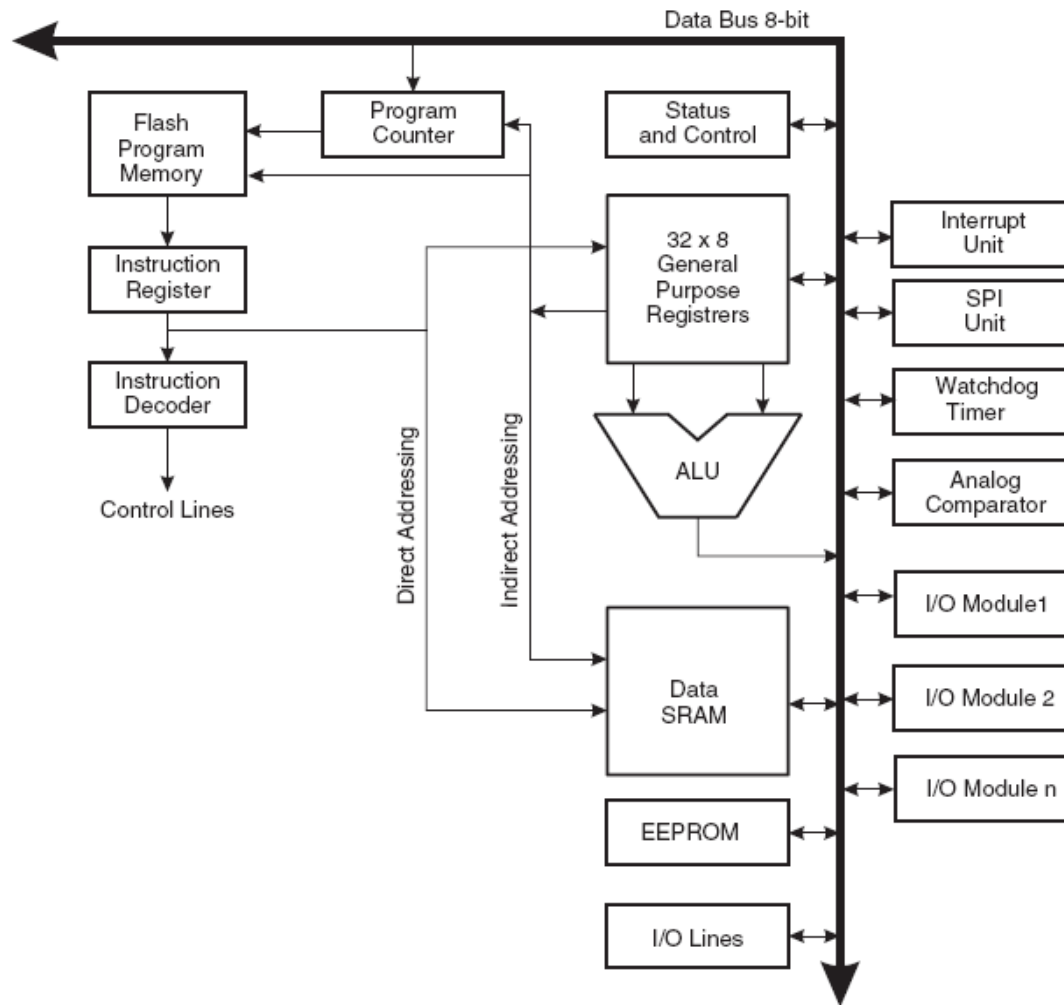
- Memory
 - 128 kb program Flash
 - 4 kb internal SRAM
 - 4 kb EEPROM
 - Optional external memory max. 64 kb
- JTAG/SPI programming interface
- Peripherals
 - 2x8-bit timer/counter
 - 2x16-bit timer /counter
 - 2x8-bit PWM output
 - 8-channel 10-bit SAR ADC

- USART
- SPI
- Watchdog timer
- Analog comparator
- Power-on reset
- Brown-down detection – supply voltage dropped below threshold -> reset uC
- Internal RC oscillator
- External and internal interrupt sources
- 6 sleep modes

- AT mega 128 inside



– Architectural overview



– General purpose registers

	7	0	Addr.	
General Purpose Working Registers	R0		\$00	
	R1		\$01	
	R2		\$02	
	...			
	R13		\$0D	
	R14		\$0E	
	R15		\$0F	
	R16		\$10	
	R17		\$11	
	...			
	R26		\$1A	X-register Low Byte
	R27		\$1B	X-register High Byte
	R28		\$1C	Y-register Low Byte
	R29		\$1D	Y-register High Byte
	R30		\$1E	Z-register Low Byte
	R31		\$1F	Z-register High Byte

– Special function registers: control or monitor chip components

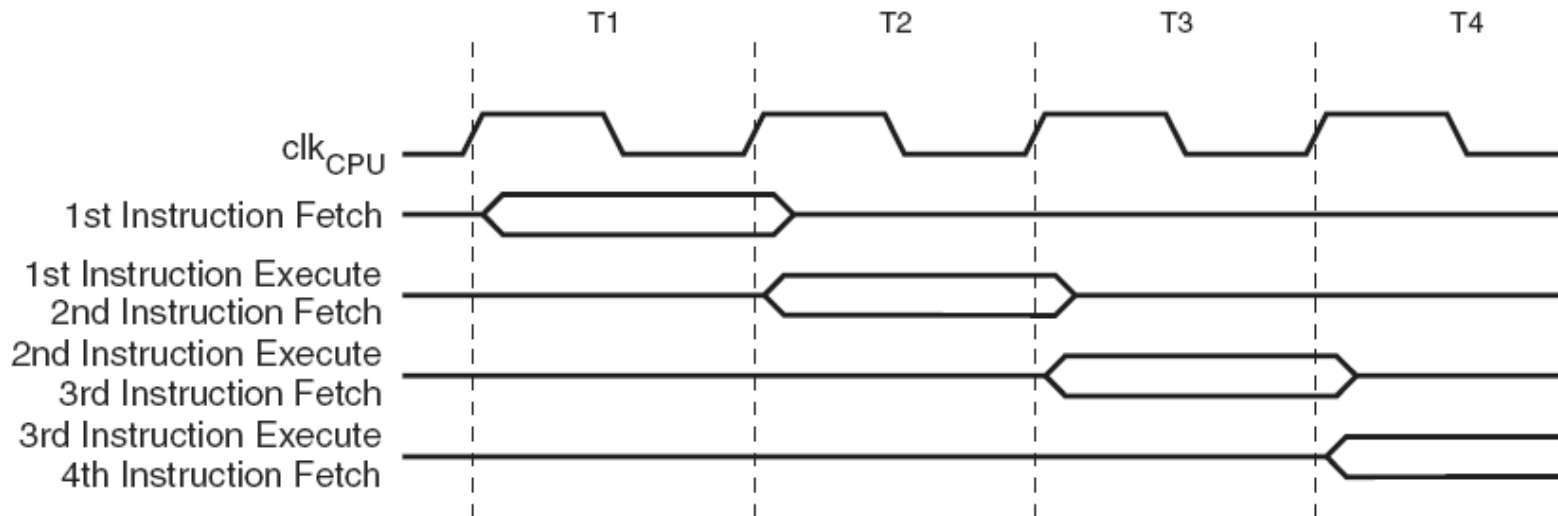
- Status register

Bit	7	6	5	4	3	2	1	0	
	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

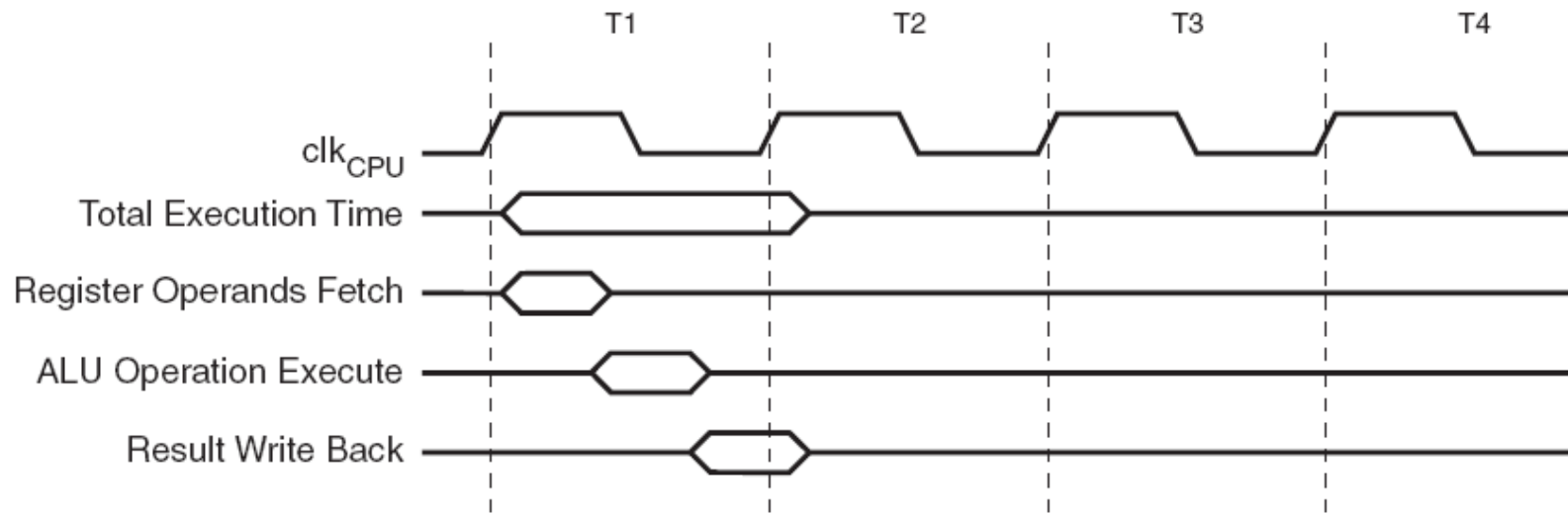
- Stack pointer

Bit	15	14	13	12	11	10	9	8	
	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SPH
	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

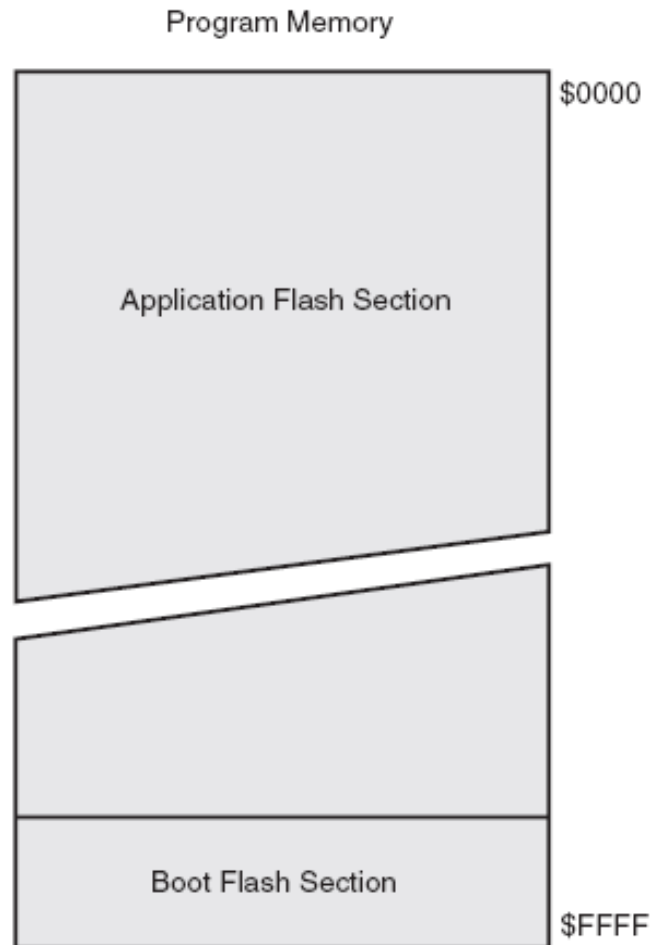
– Parallel instruction fetches and execution



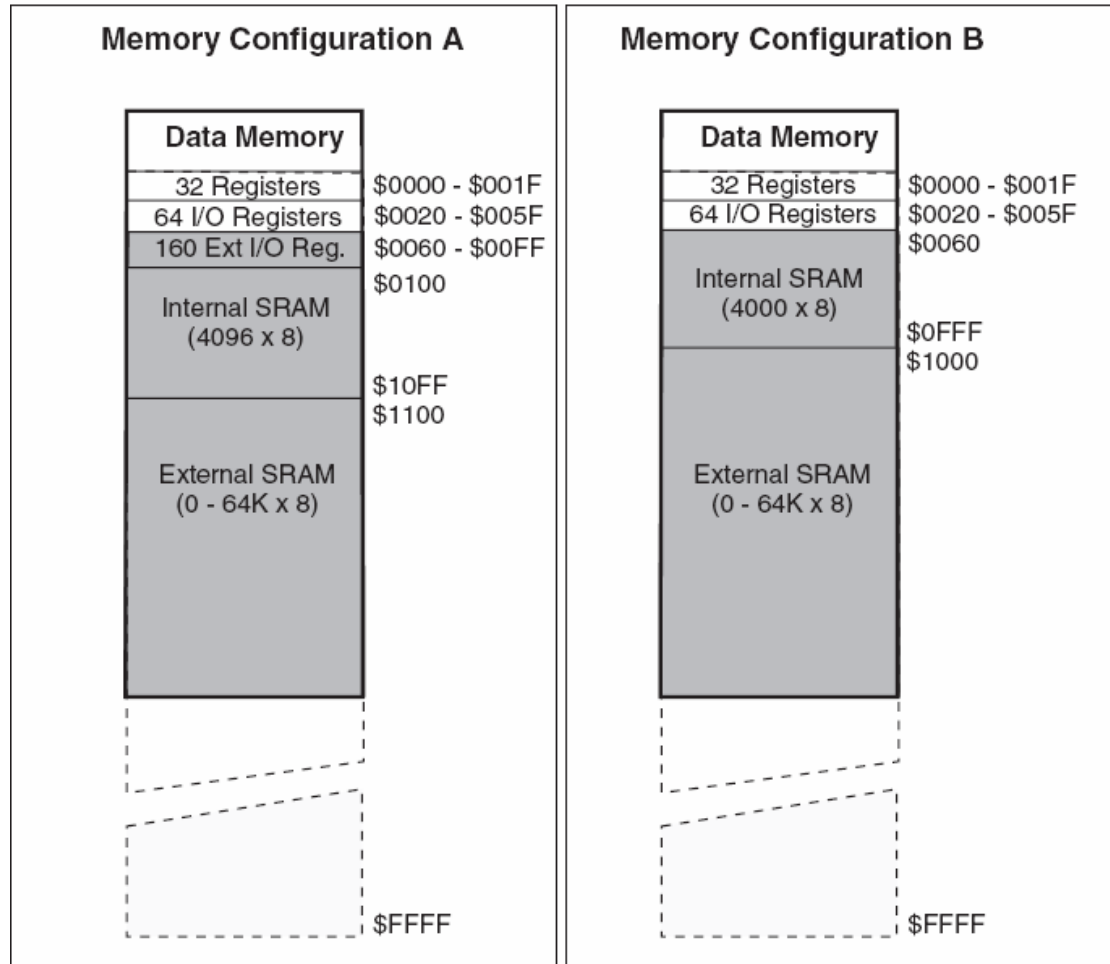
– Single cycle ALU operation



– Program memory map



- Data memory map



References

- ATMEL: 8-bit Atmel Microcontroller with 128KBytes In-System Programmable Flash
- Analog devices: Mixed signal and DSP design techniques