



BUDAPESTI MŰSZAKI ÉS GAZDASÁGTUDOMÁNYI EGYETEM
VILLAMOSMÉRNÖKI ÉS INFORMATIKAI KAR
MÉRÉSTECHNIKA ÉS INFORMÁCIÓS RENDSZEREK TANSZÉK

Digitális technika (VIMIAA03)

1. Gyakorlat & labor

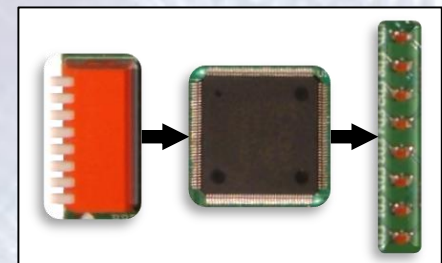
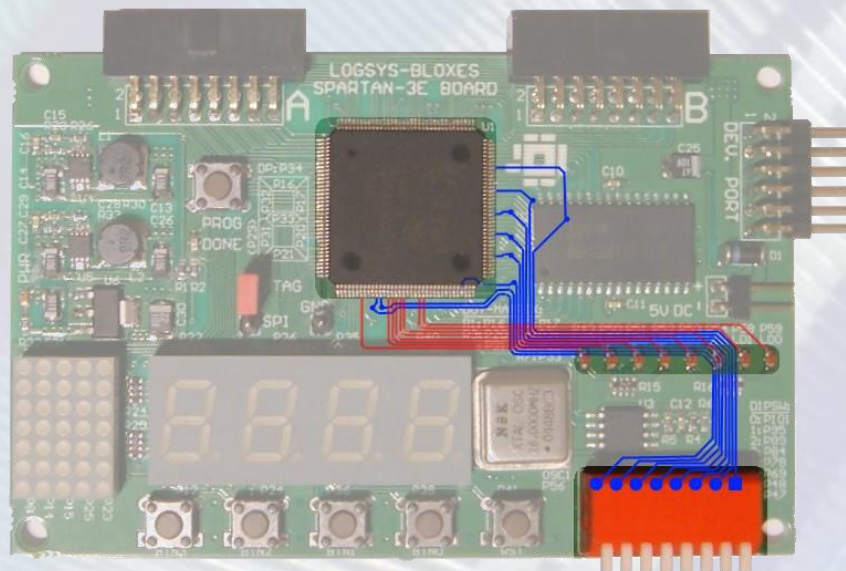
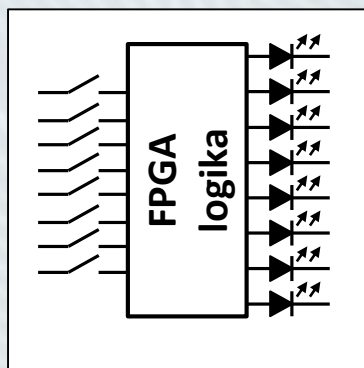
Szántó Péter

BME MIT

1. feladat: HW „Hello World!”

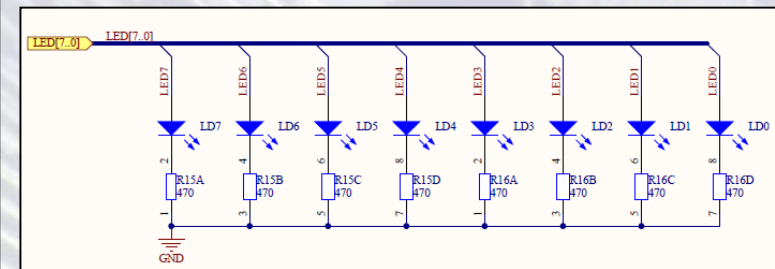
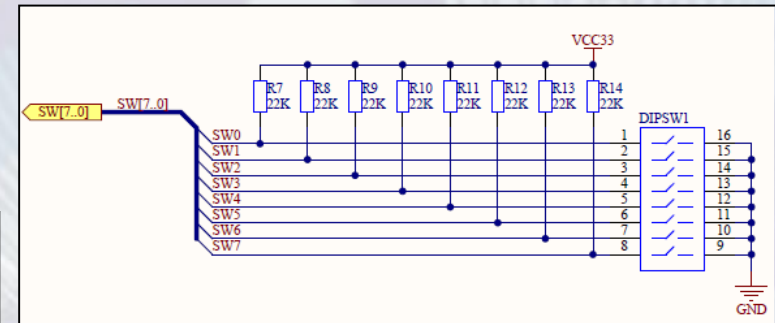
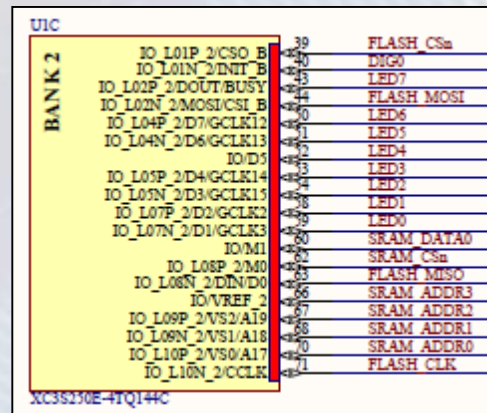
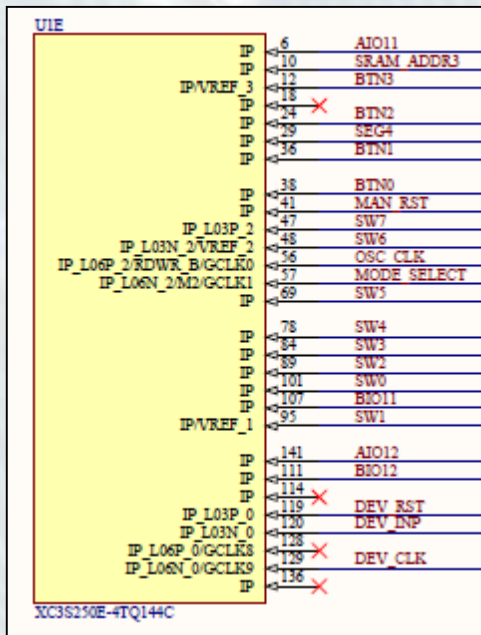
8 db LED vezérlése a 8 bites DIP kapcsolóval a LOGSYS Spartan-3E FPGA kártyán

- DIP kapcsoló → FPGA bemenet: **kék huzalozás**
- FPGA kimenet → LED: **piros huzalozás**



1.1. feladat: HW „Hello World!”

- Az elvi kapcsolási rajz a szükséges paraméterekkel (nem tananyag, csak érdeklődőknek !)

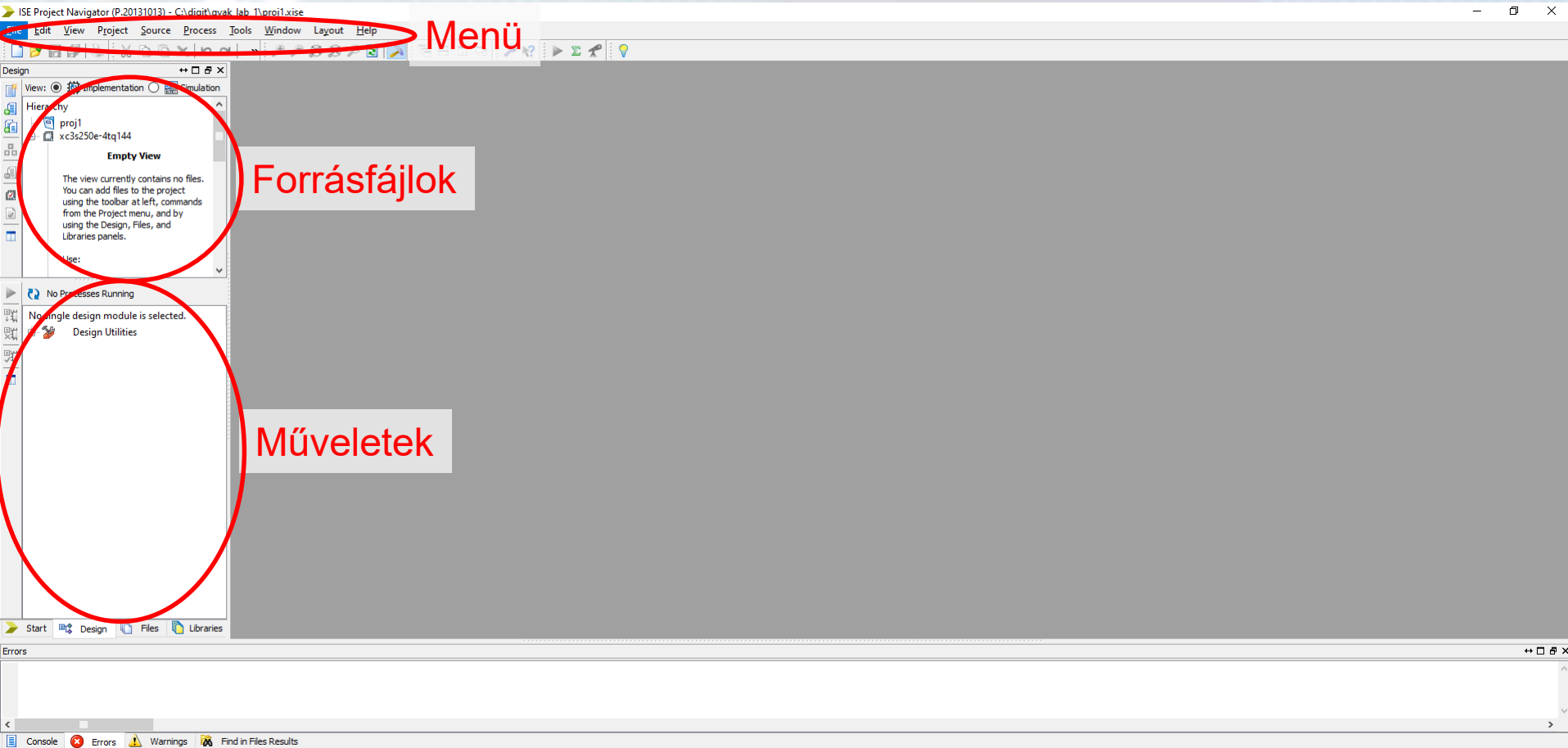


LED	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0
FPGA láb	P43	P50	P51	P52	P53	P54	P58	P59

Kapcsoló	7	6	5	4	3	2	1	0
FPGA láb	P47	P48	P69	P78	P84	P89	P95	P101

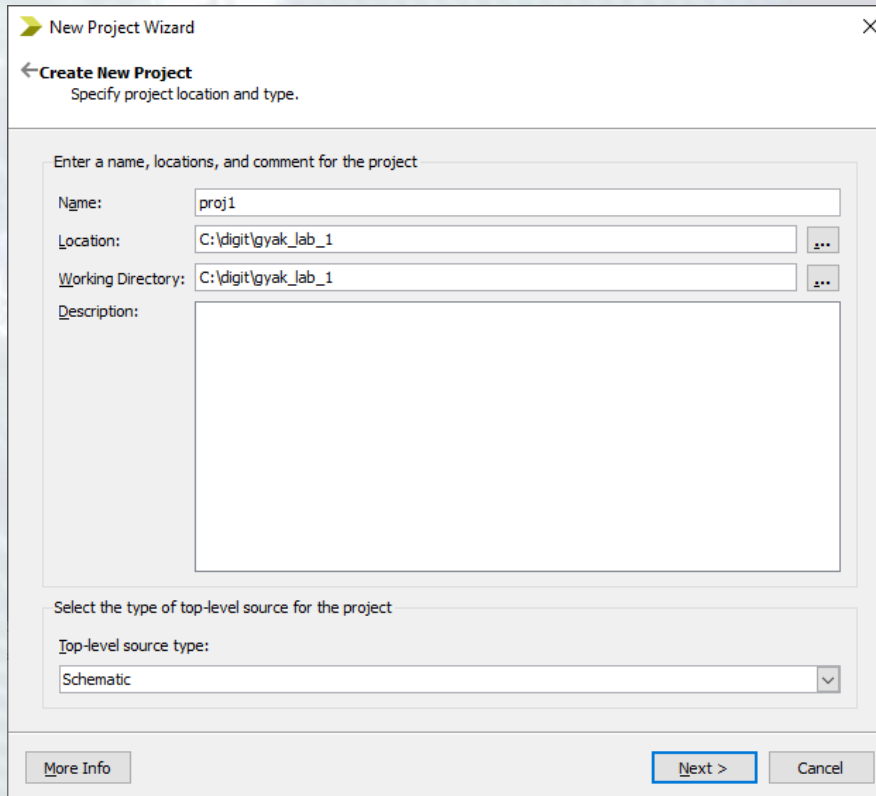
1. feladat: HW „Hello World!”

- **Xilinx ISE felhasználói felület**



1.1. feladat: HW „Hello World!”

- Projekt létrehozása



New Project Wizard

← Create New Project
Specify project location and type.

Enter a name, locations, and comment for the project

Name:

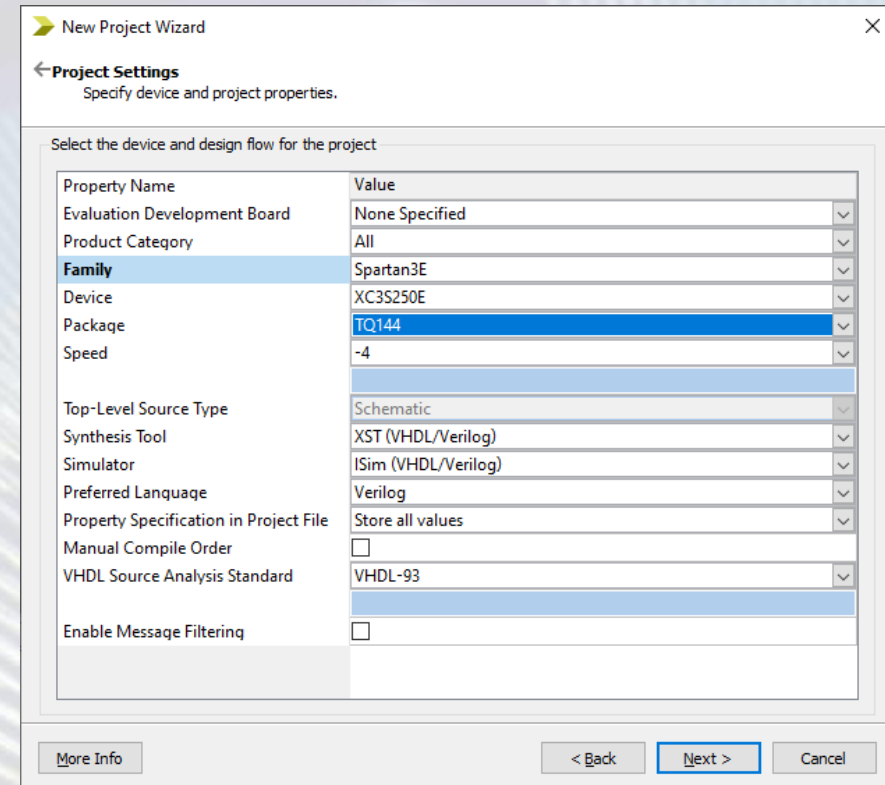
Location: ...

Working Directory: ...

Description:

Select the type of top-level source for the project

Top-level source type:



New Project Wizard

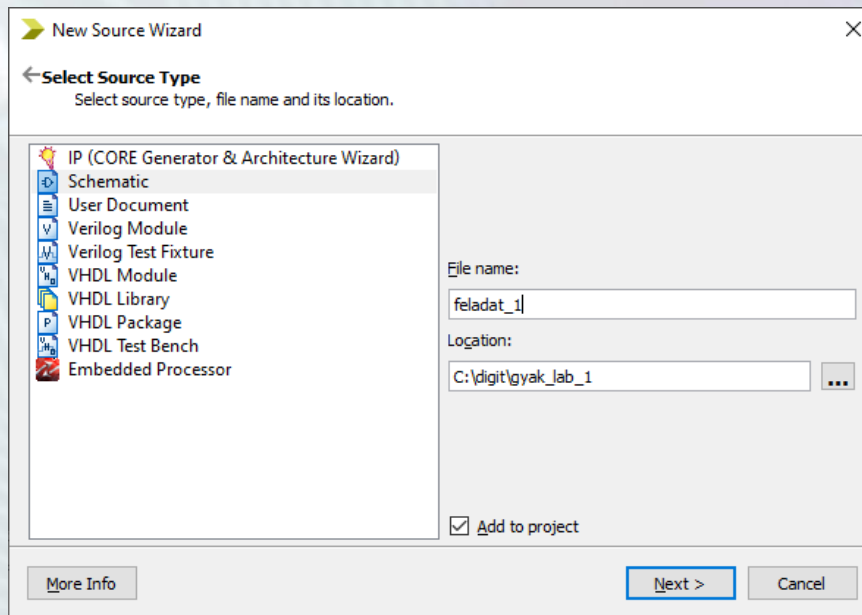
← Project Settings
Specify device and project properties.

Select the device and design flow for the project

Property Name	Value
Evaluation Development Board	None Specified
Product Category	All
Family	Spartan3E
Device	XC3S250E
Package	TQ144
Speed	-4
Top-Level Source Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

1.1. feladat: HW „Hello World!”

- **Kapcsolási rajz forrásfájl hozzáadása: “Schematic”**



1.1. feladat: HW „Hello World!”

- **Kapcsolási rajz szerkesztő felület**

Vezeték

I/O Marker: ki- és bemenetek jelölés

Kapcsolási rajz szimbólumok

```
Started : "Creati...
Running createsch...
Command Line: createsch -intstyle ise -family spartan3e C:/digit/gyak_lab_1/feladat_1.sch

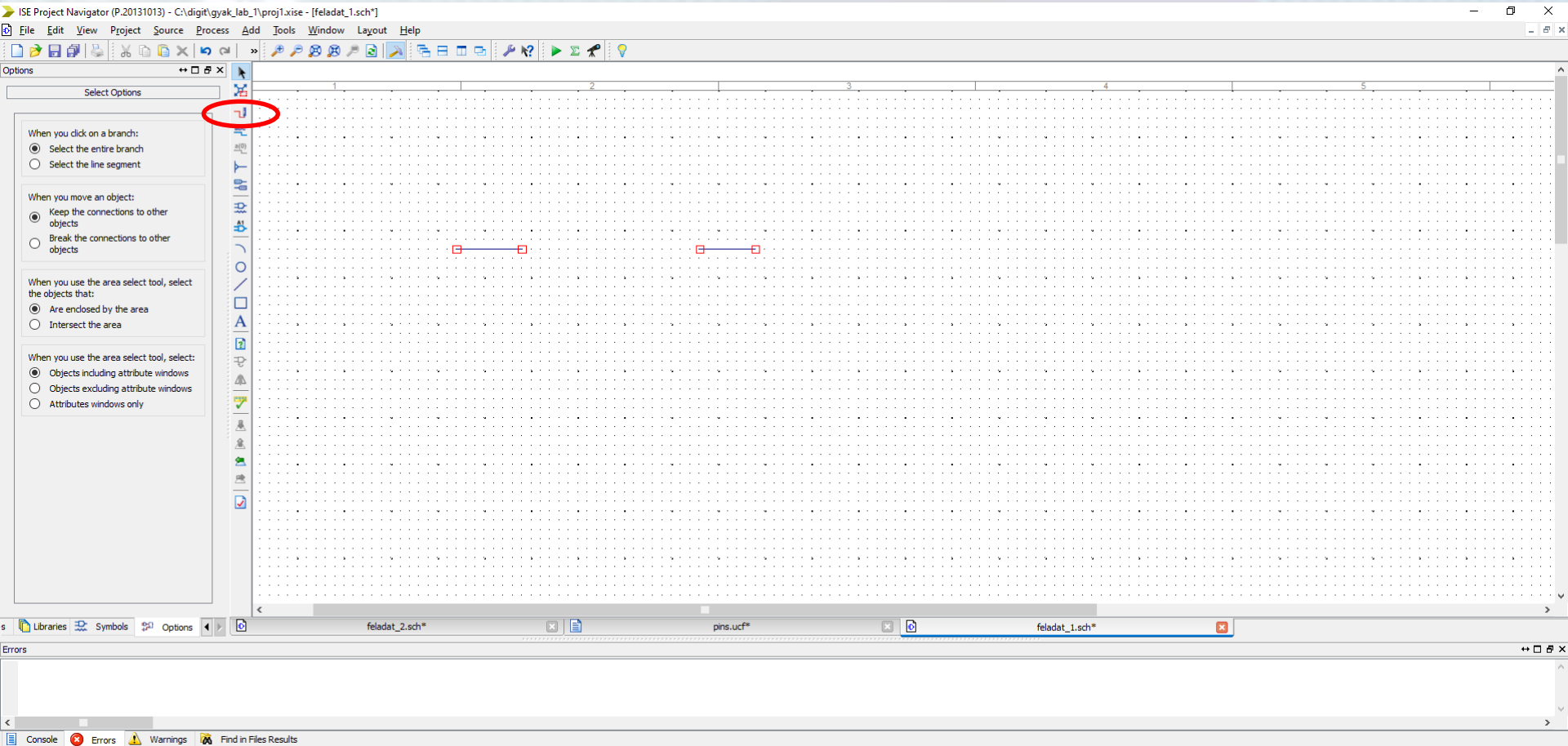
Process "Creating Schematic" completed successfully

Started : "Launching Schematic Editor to edit feladat_1.sch".
Launching Design Summary/Report Viewer...
```

[2796,1568]

1.1. feladat: HW „Hello World!”

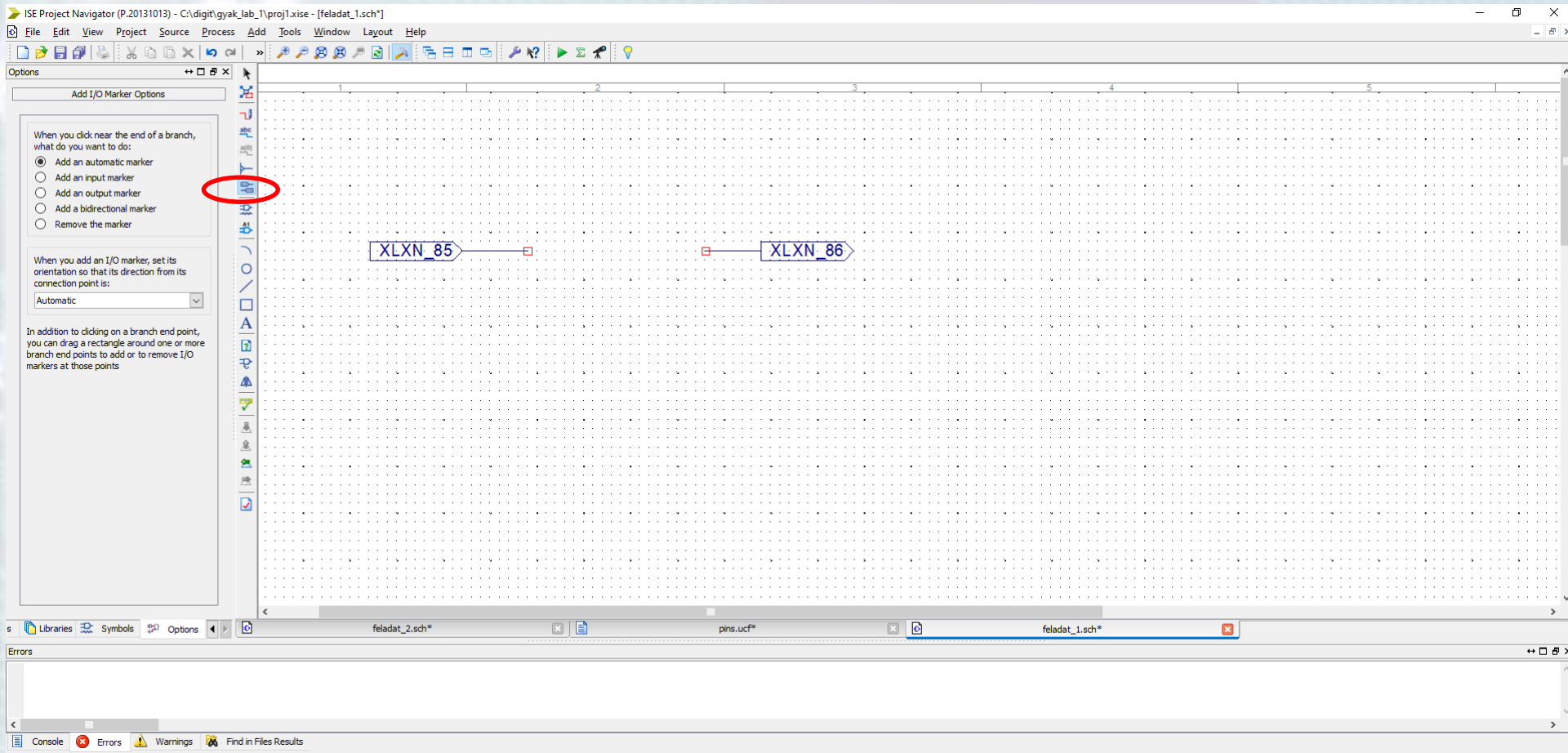
- Vezetékek hozzáadása



[2200,656]

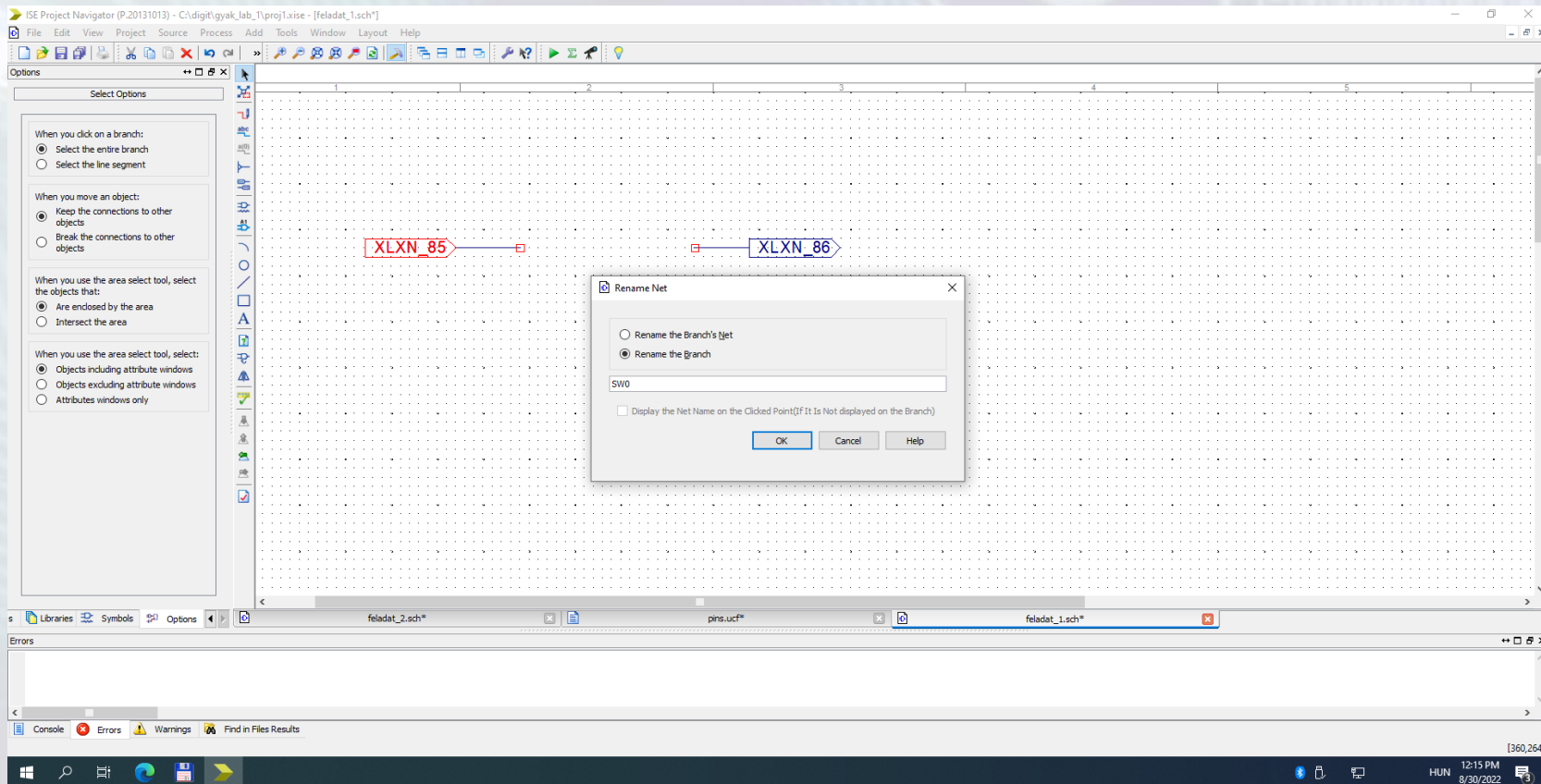
1.1. feladat: HW „Hello World!”

- I/O Marker-ek hozzáadása



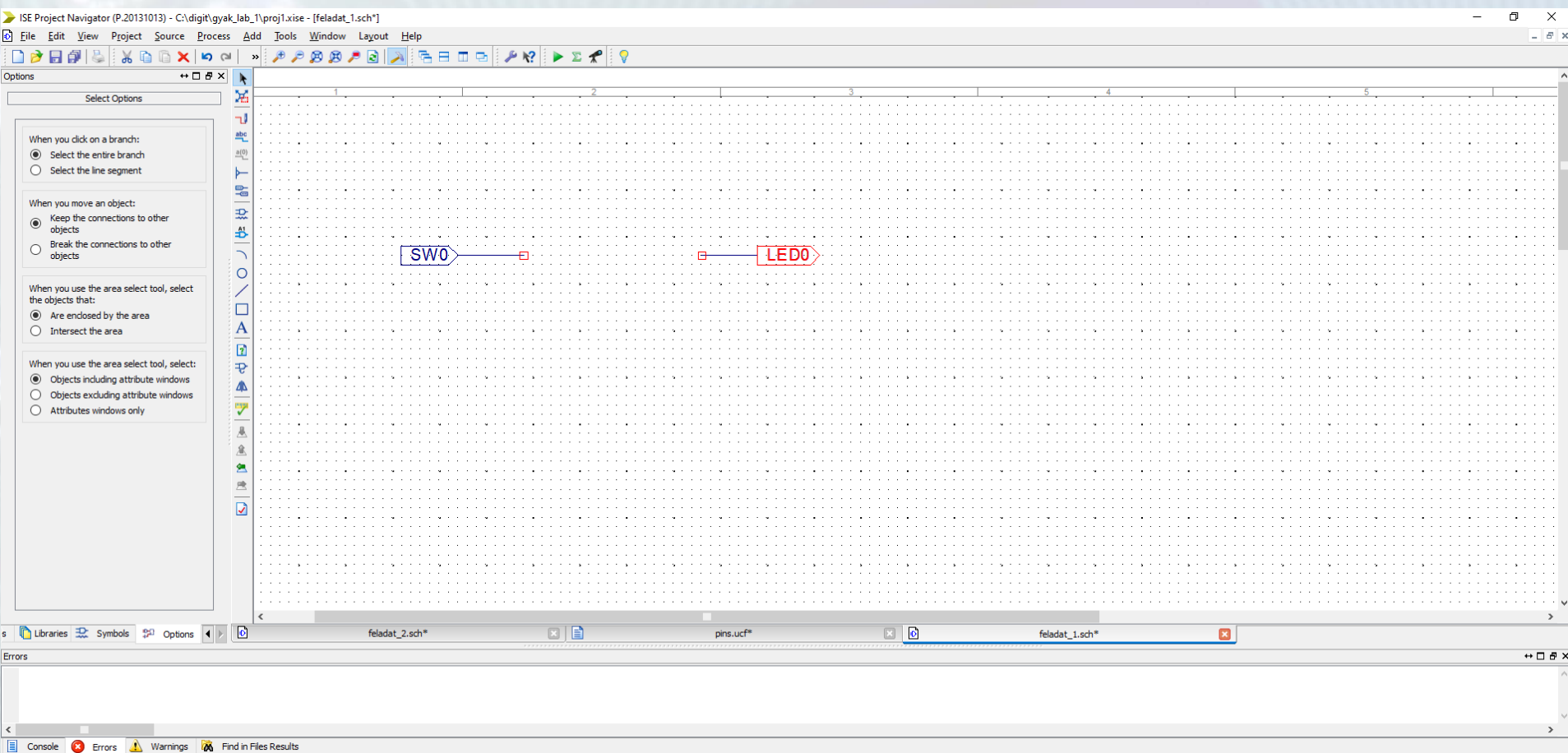
1.1. feladat: HW „Hello World!”

- I/O Marker átnevezése
 - Jobb klikk az I/O Marker-en, majd “Rename Port”



1.1. feladat: HW „Hello World!”

- SW0 és LED0 I/O Marker-ek



[1164,-48]

1.1. feladat: HW „Hello World!”

- **SW0 és LED0 nem köthető össze egyszerűen egy vezetékkel**
 - ISE követelmény
- **Kell közük valamilyen szimbólum**
 - IBUF és OBUF
 - Speciális FPGA elemek a ki- és bemenetekhez, logikailag nem csinál semmit

1.1. feladat: HW „Hello World!”

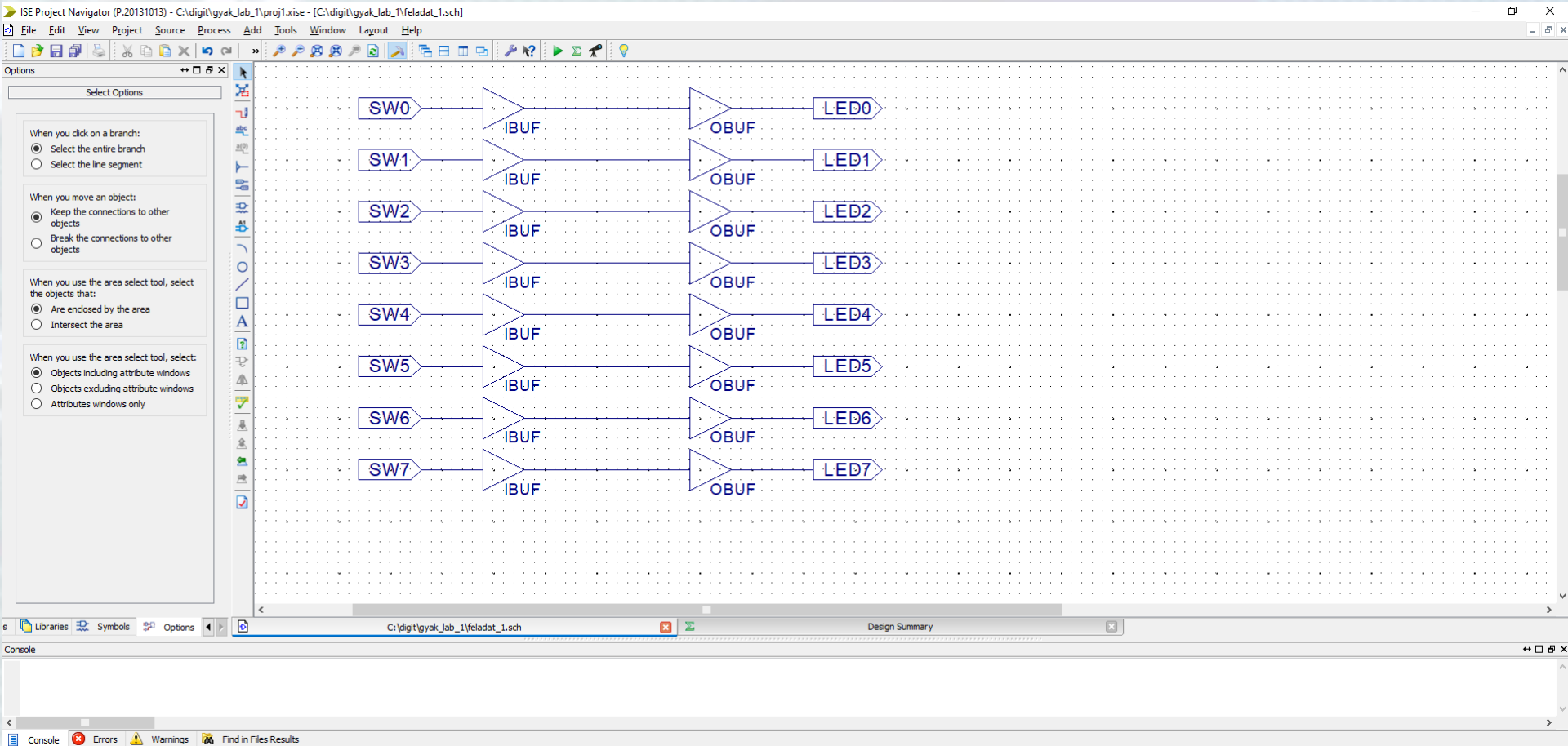
- **IBUF és OBUF szimbólum hozzáadása**

The screenshot displays the Xilinx ISE Project Navigator interface. The main workspace shows a logic diagram on a grid. The diagram consists of four components connected in a sequence: a switch labeled 'SW0', an input buffer labeled 'IBUF', an output buffer labeled 'OBUF', and an LED labeled 'LED0'. The connections are as follows: SW0 is connected to the input of IBUF, IBUF is connected to the input of OBUF, and OBUF is connected to LED0. On the left side, the 'Symbols' panel is open, showing a list of categories and a search filter set to 'obuf'. The search results list various buffer symbols: obuf, obuf16, obuf4, obuf8, obufds, obuft, obuft16, obuft4, obuft8, and obuftds. The bottom status bar shows the current project name 'feladat_1.sch*' and the current component 'pins.ucf'.

[1340;-36]

1.1. feladat: HW „Hello World!”

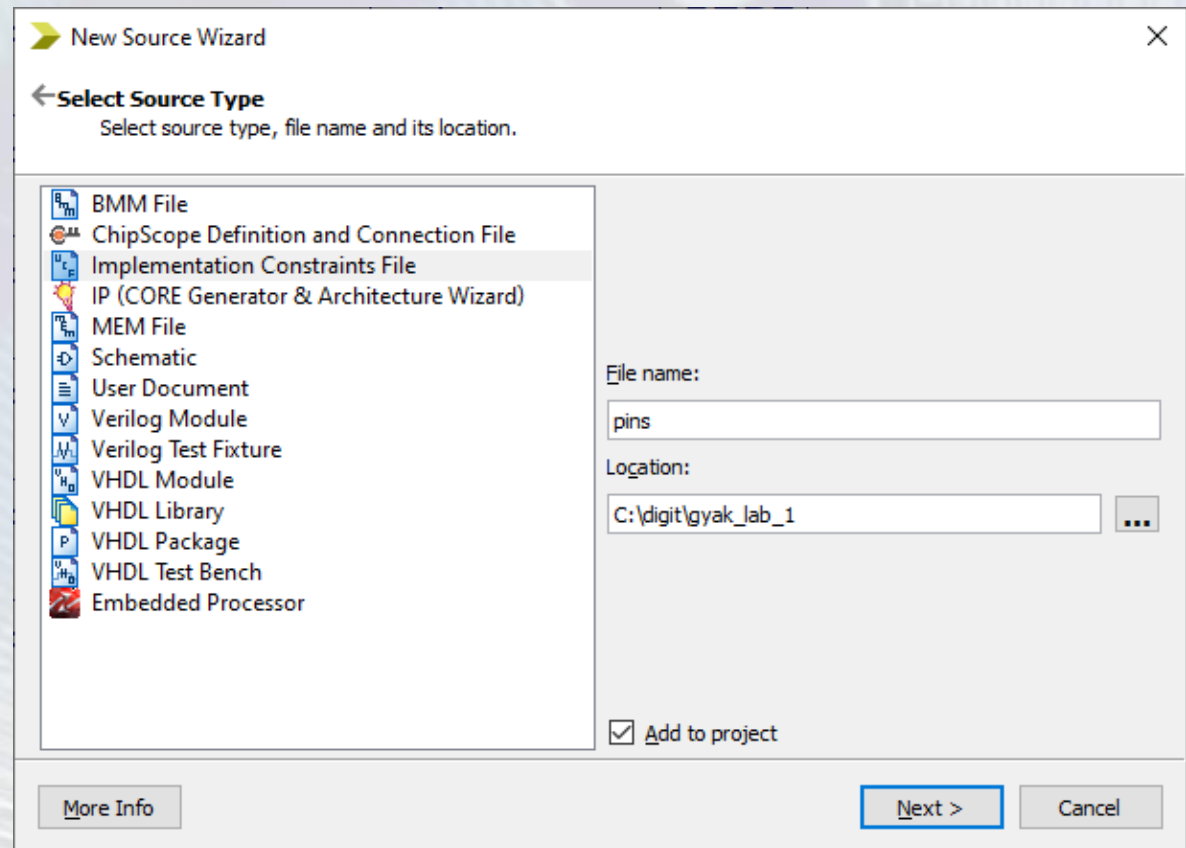
- 8 kapcsoló összekötése a 8 LED-del



[1256,1244]

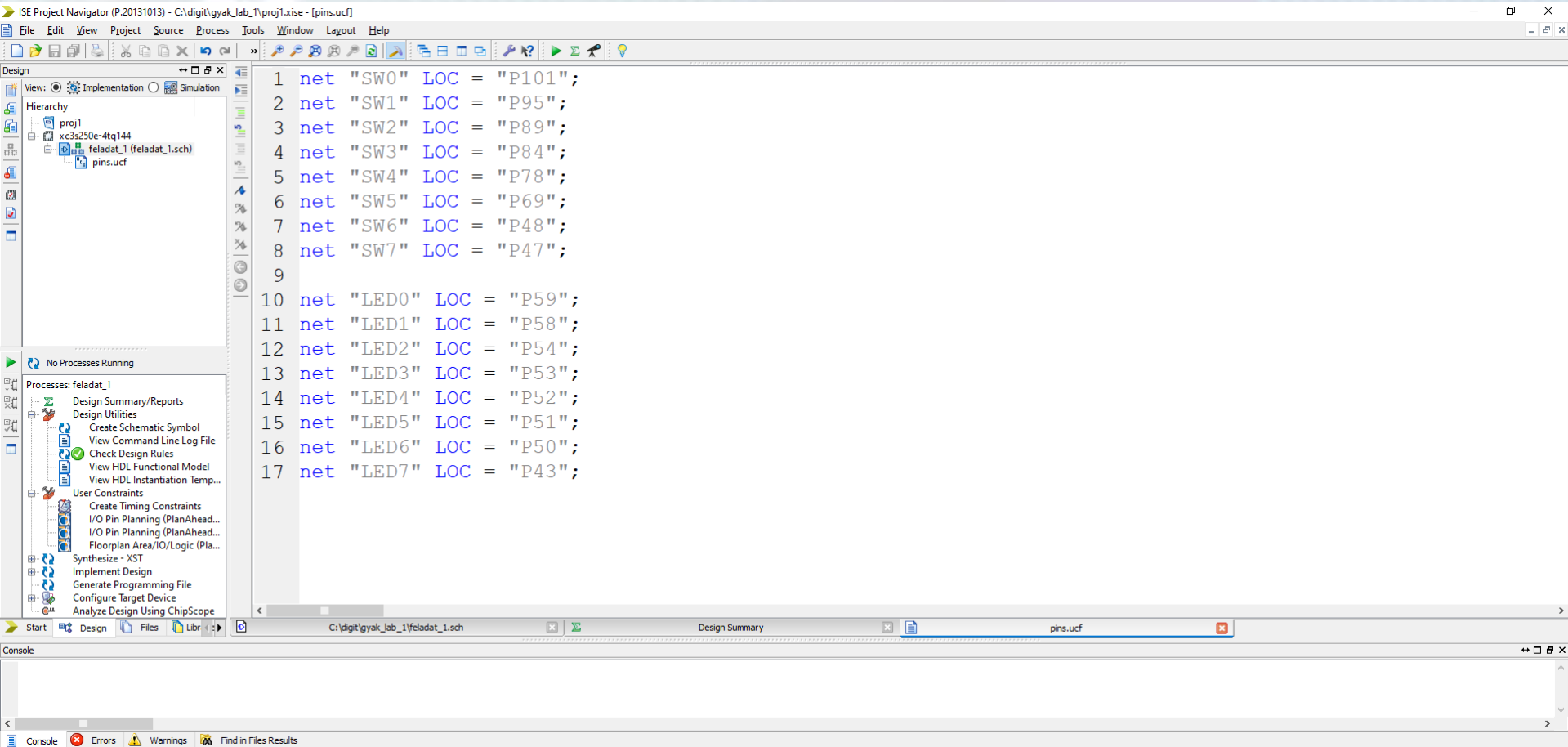
1.1. feladat: HW „Hello World!”

- I/O portok (I/O Maerker-ek) hozzárendelése az FPGA fizikai lábaihoz: **Implementation Constraint File**



1.1. feladat: HW „Hello World!”

- Constraint File tartalma a kapcsolási rajz alapján:



The screenshot shows the ISE Project Navigator interface. The main window displays the contents of the Constraint File (pns.ucf) for the project 'proj1'. The file contains 17 net definitions, each with a unique name and a location (LOC). The nets are:

```
1 net "SW0" LOC = "P101";
2 net "SW1" LOC = "P95";
3 net "SW2" LOC = "P89";
4 net "SW3" LOC = "P84";
5 net "SW4" LOC = "P78";
6 net "SW5" LOC = "P69";
7 net "SW6" LOC = "P48";
8 net "SW7" LOC = "P47";
9
10 net "LED0" LOC = "P59";
11 net "LED1" LOC = "P58";
12 net "LED2" LOC = "P54";
13 net "LED3" LOC = "P53";
14 net "LED4" LOC = "P52";
15 net "LED5" LOC = "P51";
16 net "LED6" LOC = "P50";
17 net "LED7" LOC = "P43";
```

The interface also shows a Hierarchy view on the left and a Process list at the bottom left. The Process list includes various design steps such as 'Design Summary/Reports', 'Design Utilities', 'User Constraints', and 'Synthesize - XST'.

1.1. feladat: HW „Hello World!”

- Terv implementálása

The screenshot displays the Xilinx ISE Project Navigator interface. The main workspace shows a logic diagram with eight switches (SW0 to SW7) connected to eight LEDs (LED0 to LED7) through a chain of buffers (IBUF and OBUF). The left sidebar contains a project hierarchy and a list of processes. The 'Generate Programming File' process is highlighted with a red circle and a red arrow pointing to the text 'Generate Programming File' overlaid on the diagram. The console window at the bottom shows the following output:

```
Process "Generate Post-Place & Route Static Timing" completed successfully
Started : "Generate Programming File".
Running bitgen...
Command Line: bitgen -intstyle ise -f feladat_1.ut feladat_1.ncd
Process "Generate Programming File" completed successfully
Launching "View/Edit Routed Design (FPGA Editor)"...
```

[548,500]

1.1. feladat: HW „Hello World!”

- Kipróbálás hardveren

The screenshot displays the Logsys Control Panel software interface. The main window is titled "Logsys Control Panel" and contains several sections:

- Info:** LOGSYS development cable
- Control:** RST, CLK (10 Hz), and a "Set" button.
- Power:** A "+5V On" button (indicated by red arrow 1), Current Maximum Value (450 mA), and a "Log to file..." checkbox.
- Measurement:** +5Vout (4,94 V), I/Oref (3,31 V), JTAGref (2,51 V), Maximum Value (500 mA), Critical Value (90 %), and Samples/Second (10).
- Configuration:** JTAG Download (checked), BitBang I/O, UART, and USRT.
- Communication:** BitBang I/O, UART, and USRT.
- Download (DC023):** A "Query JTAG chain" button (indicated by red arrow 3), a dropdown menu showing "XC3S250E (Xilinx)", and a "Configure the selected device..." button (indicated by red arrow 4).
- Log:** A text area showing "Found 1 device(s) in the JTAG chain." and a "Clear Log" button.
- Bottom Panel:** A gauge showing current measurement with a needle pointing to 045,00 mA (indicated by red arrow 2) and a scale from 0 to 500,00 mA.

1.2. feladat: Busz használata

- **Busz: “több vezeték együttese”**
 - 8 bites busz: 8 darab vezeték
- **Feladat megvalósítása busszal**
 - A 8 darab “I/O Marker → IBUF → vezeték → OBUF → I/O Marker” helyett
 - Egy darab 8 bites “I/O Marker → IBUF → vezeték → OBUF → I/O Marker”
 - IBUF8 és OBUF8

1.2. feladat: Busz használata

- **Kapcsolási rajz és busz átnevezése**

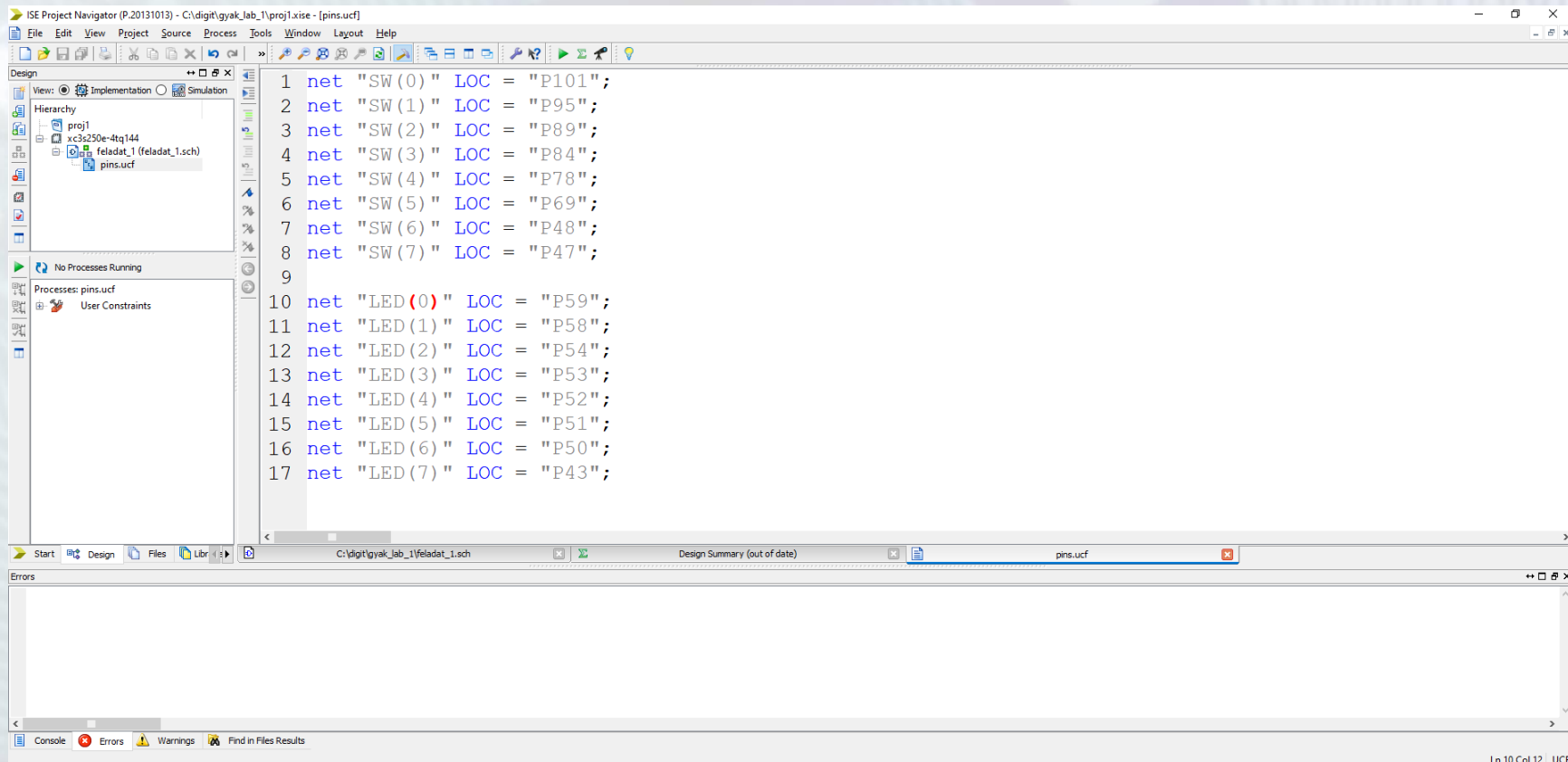
The screenshot displays the Xilinx ISE Project Navigator interface. The main workspace shows a schematic diagram with a signal path from a switch **SW(7:0)** through an **IBUF8** input buffer, followed by an **OBUF8** output buffer, and finally to an LED **LED(7:0)**. The signal is represented by a blue bus line.

On the right side, the **Rename Bus** dialog box is open. It contains the following elements:

- Rename the branch's bus** (selected radio button) and **OK** button.
- Rename the branch** (unselected radio button) and **Help** button.
- Current Base Name of Bus**: `XLXN_71`
- New Base Name of Bus**: `LED` (circled in red).
- Apply** button (circled in red).
- Related buses and nets** list:
 - 1
 - `XLXN_71(7:0)` (highlighted in blue and circled in red)
- Select All** and **Clear All** buttons.
- Highlight** section:
 - `XLXN_71(7:0)` (expanded)
 - `Sheets`
 - `Pins`
 - Center**, **Zoom In**, and **Zoom Out** buttons.

1.2. feladat: Busz használata

- **Constraint fájl módosítása: busz (SW és LED) egyes bitjeinek kiválasztása: ()**



```
ISE Project Navigator (P.20131013) - C:\digit\gyak_lab_1\proj1.xise - [pins.ucf]
File Edit View Project Source Process Tools Window Layout Help

Design
View: Implementation Simulation
Hierarchy
proj1
  xc3s250e-4tq144
    feladat_1 (feladat_1.sch)
      pins.ucf
No Processes Running
Processes: pins.ucf
  User Constraints

1 net "SW (0)" LOC = "P101";
2 net "SW (1)" LOC = "P95";
3 net "SW (2)" LOC = "P89";
4 net "SW (3)" LOC = "P84";
5 net "SW (4)" LOC = "P78";
6 net "SW (5)" LOC = "P69";
7 net "SW (6)" LOC = "P48";
8 net "SW (7)" LOC = "P47";
9
10 net "LED (0)" LOC = "P59";
11 net "LED (1)" LOC = "P58";
12 net "LED (2)" LOC = "P54";
13 net "LED (3)" LOC = "P53";
14 net "LED (4)" LOC = "P52";
15 net "LED (5)" LOC = "P51";
16 net "LED (6)" LOC = "P50";
17 net "LED (7)" LOC = "P43";

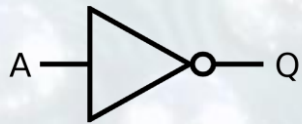
C:\digit\gyak_lab_1\feladat_1.sch Design Summary (out of date) pins.ucf
Errors
Ln 10 Col 12 | UCF
```

1.2. feladat: Busz használata

- **Konfigurációs fájl generálása**
 - ISE: “Generate Configuration fájl”
- **Kipróbálás hardveren**
 - FPGA programozás LOGSYS GUI-val

2. feladat: Logikai műveletek

Inverter



A	Q
0	1
1	0

AND



A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NAND



A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

OR



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

NOR



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

XOR



A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

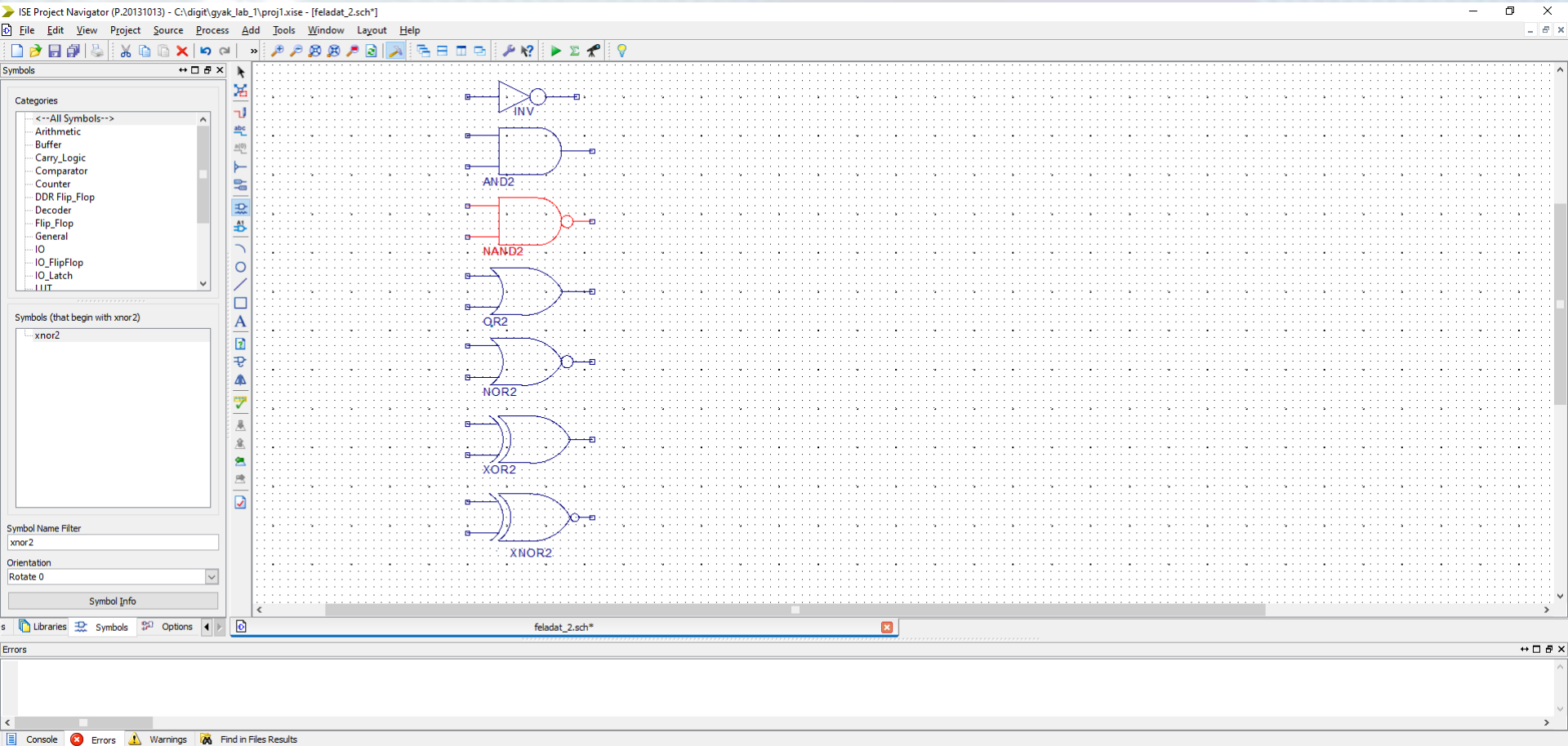
XNOR



A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

2. feladat: Logikai műveletek

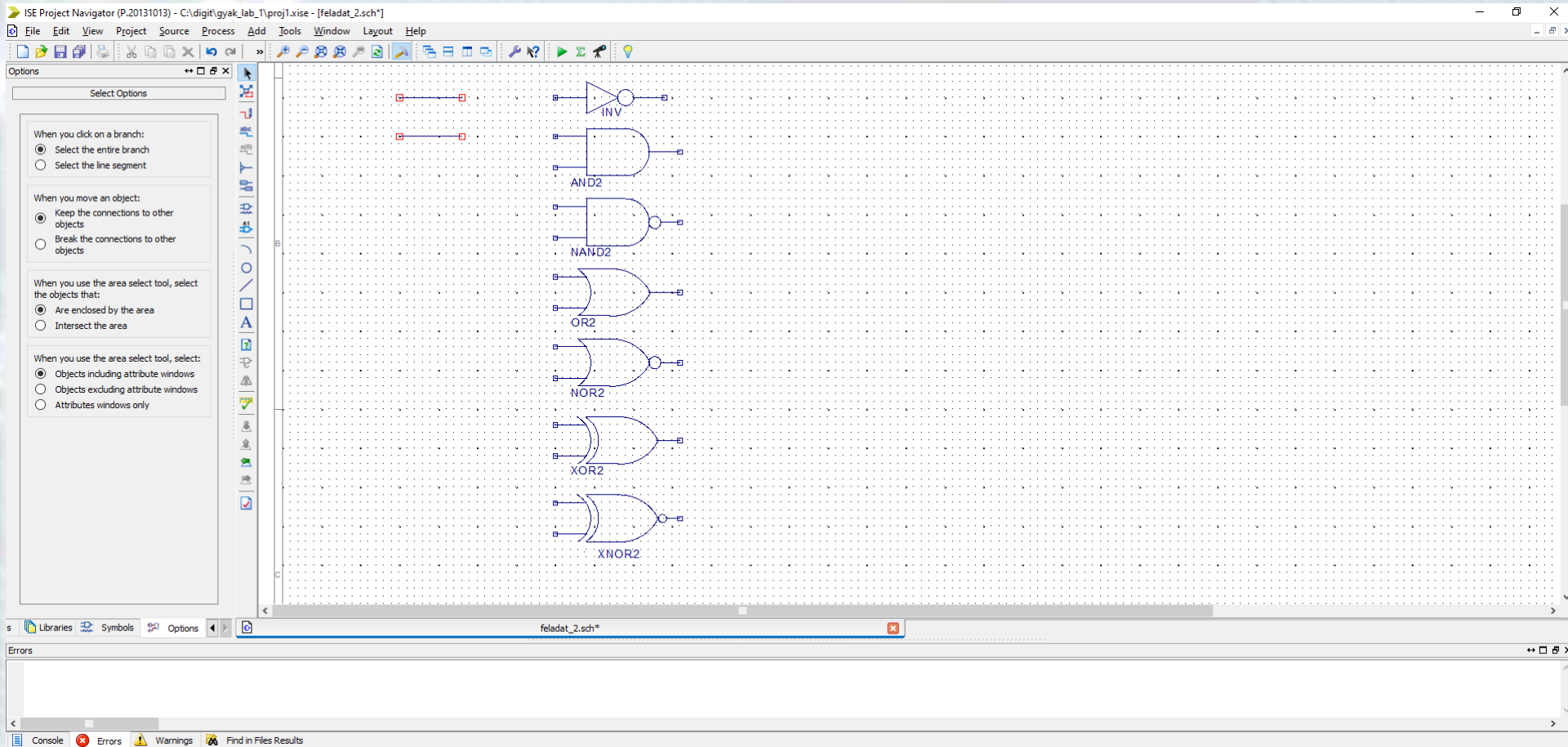
- Szimbólumok hozzáadása



[1748,688]

2. feladat: Logikai műveletek

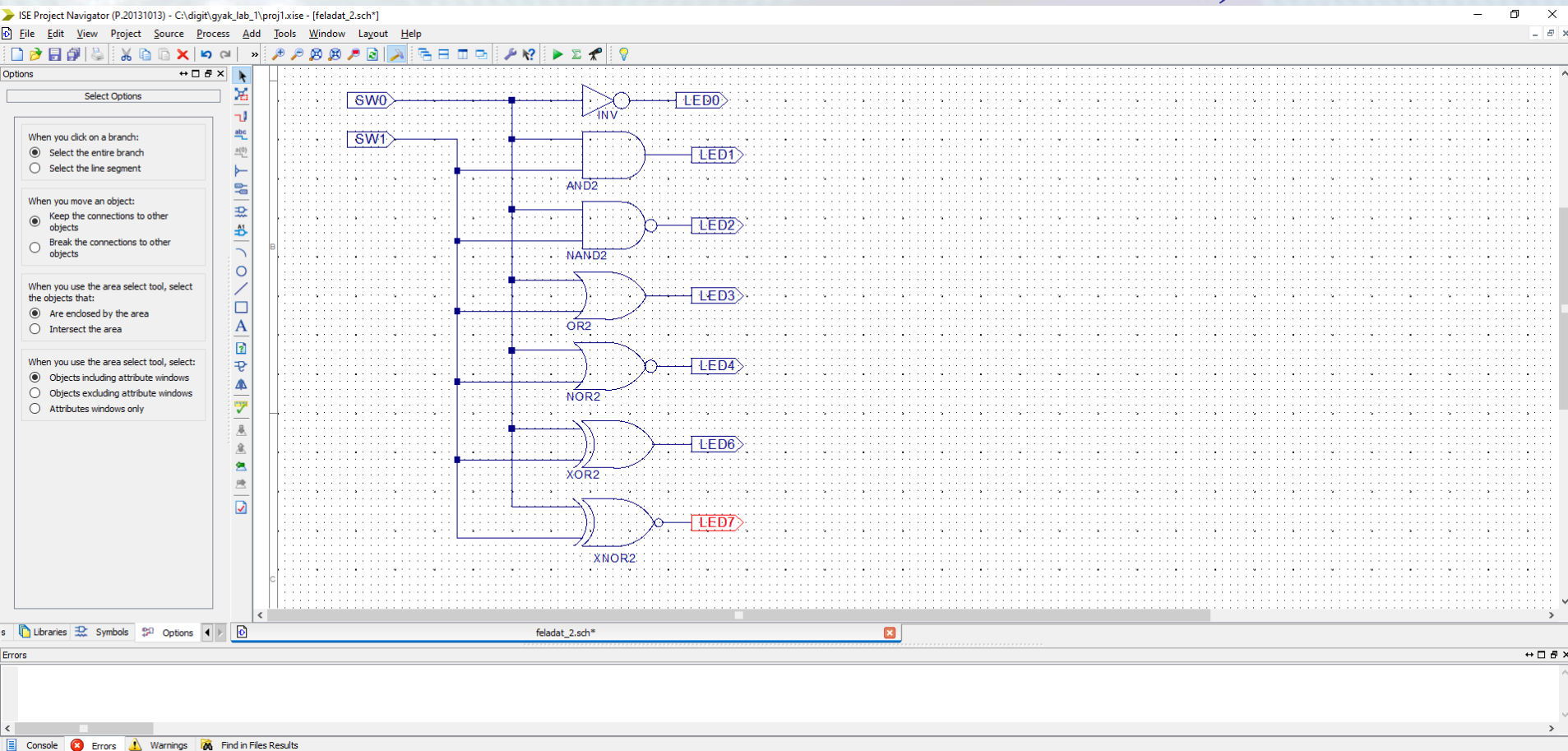
- Vezetékek hozzáadása



[712,652]

2. feladat: Logikai műveletek

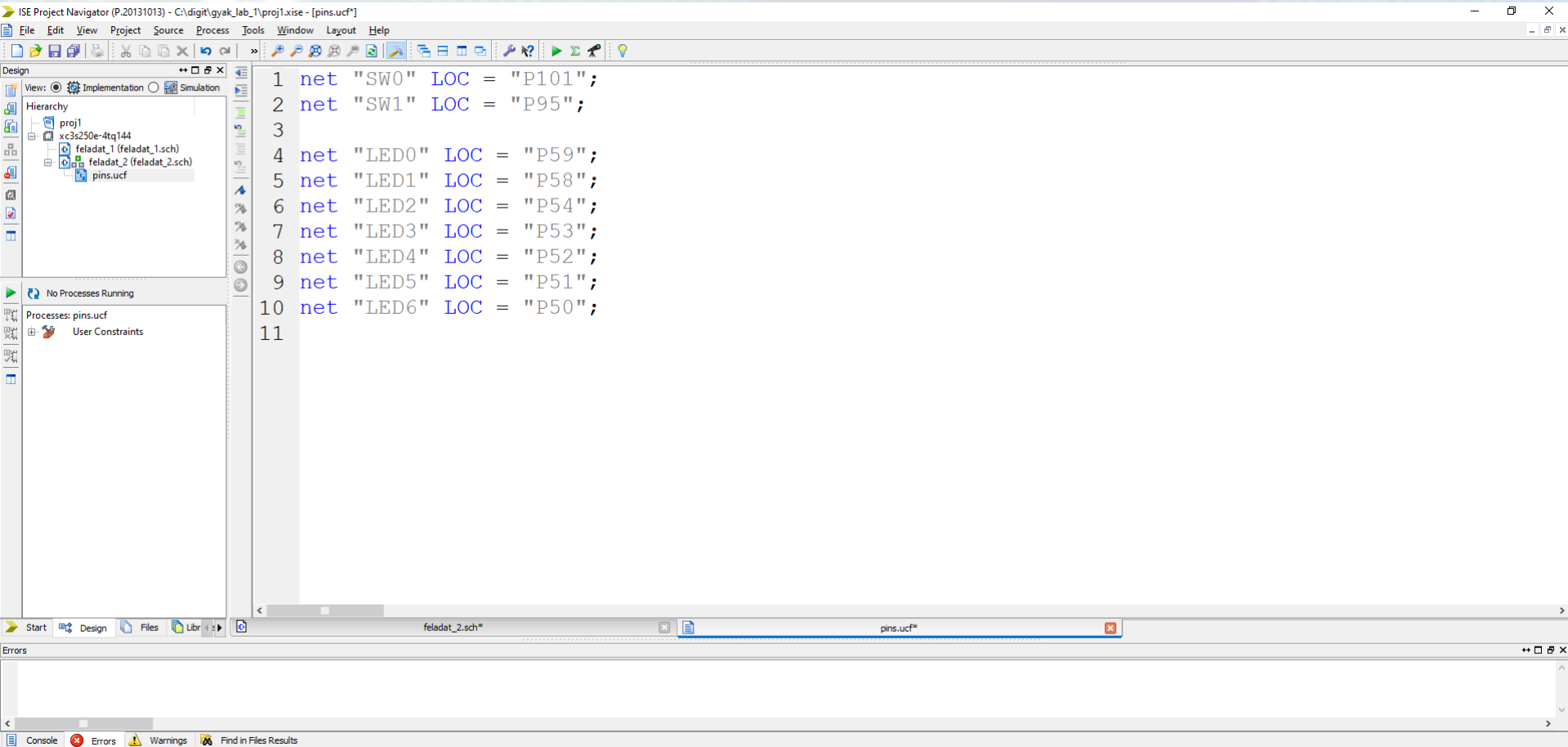
- I/O Marker-ek hozzáadása és átnevezése, összekötése



[576,656]

2. feladat: Logikai műveletek

- Constraint fájl módosítása



The screenshot shows the Xilinx ISE Project Navigator interface. The main window displays the content of the 'pins.ucf' constraint file, which contains 11 lines of net constraints. The left sidebar shows the project hierarchy with 'proj1' containing 'xc3s250e-4tq144', 'feladat_1 (feladat_1.sch)', 'feladat_2 (feladat_2.sch)', and 'pins.ucf'. The bottom status bar indicates 'Ln 10 Col 10 UCF'.

```
1 net "SW0" LOC = "P101";
2 net "SW1" LOC = "P95";
3
4 net "LED0" LOC = "P59";
5 net "LED1" LOC = "P58";
6 net "LED2" LOC = "P54";
7 net "LED3" LOC = "P53";
8 net "LED4" LOC = "P52";
9 net "LED5" LOC = "P51";
10 net "LED6" LOC = "P50";
11
```

2. feladat: Logikai műveletek

- **Konfigurációs fájl generálása**
 - “Generate Configuration fájl”
- **Kipróbálás hardveren**
 - FPGA programozás LOGSYS GUI-val