CHAPTER 7

Internal structure of operational amplifiers

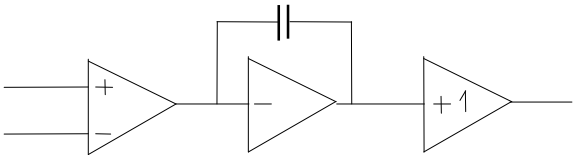
1. Classifications:

- according to technology: bipolar
  BiFET, BiMOS
  MOSFET

- according to application: universal (or general purpose),
  fast (high f_{lh} and SR = slew rate),
  precision (small offset),
  small supply current ($I_{supply} < 0.1$ mA),
  small supply voltage,
  small input current,
  small noise,
  single supply,
  etc.

2. General structure:

- universal

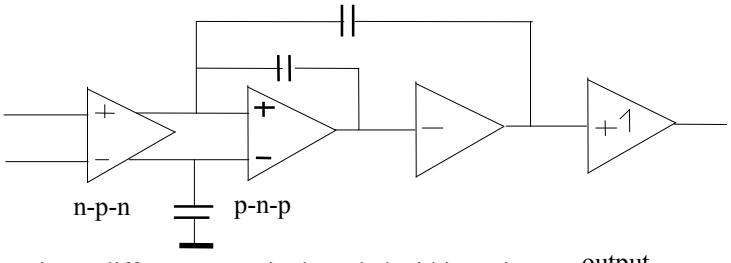


input diff amp.
big CMRR
offset setting
phase addition
big R_{ind}, R_{inc}
and R_{vd1}

main amp.
big A_v (CE)
frequency-
compensation

power stage
compl. E-fol-
lower; current
limiting
small R_{out}

-fast

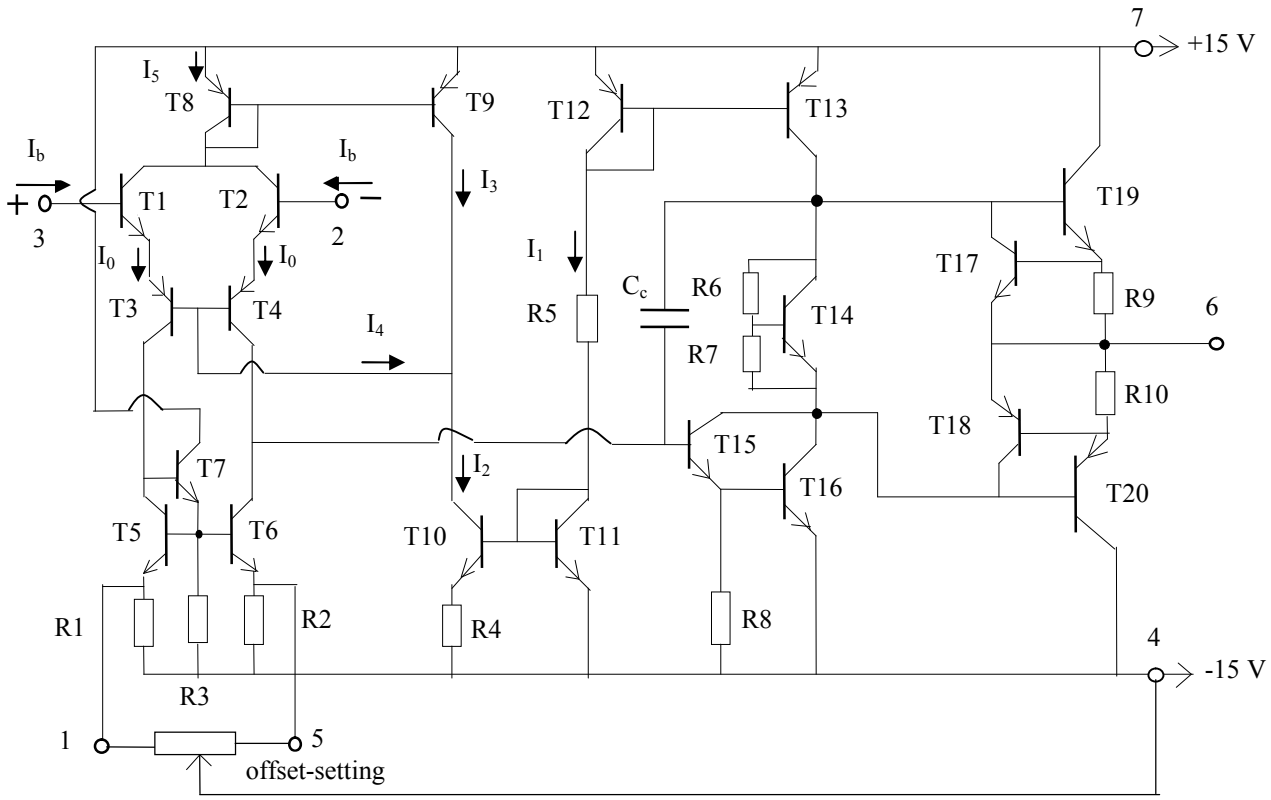


input diff.
amp.

single ended within main
ampl.; sophisticated
frequency-compensation

output
similar to
universal

Example: the type 741, bipolar universal operational amplifier



Operation points:

The T12 - R5 - T11 is the input leg of two current mirrors:

1. the T11 - T10 and T9 - T8 current mirrors set the operation point current of the input differential amplifier,
2. the T12 - T13 current mirror sets the operation point current of the CE main amplifier with a Darlington pair of transistors.

The I_1 current of the input leg (R5 = 39 k): $I_1 = (2 \cdot 15 - 2 \cdot 0{,}6)/39 = 0.7$ mA

1. The output of the T11 - T10 current mirror with decreasing transfer (because of R4 = 5 k): $I_2 =$ 35 µA. A part of this is the total base current of transistors T3, T4: $I_4 = 5$ µA, the remaining part $I_3 = I_5 = 30$ µA providing the total op. point current of the input stage, thus the current of two legs of the diff. amplifier: $I_0 = I_5/2 = 15$µA.
This combined with the bias current given by the catalogue as $I_b = 100$ nA gives the current gain of the input transistors T1 and T2: ß ~ B = 15 000/100 = 150.

2. Towards the main amplifier the current transfer is 1:1, thus the op. point current of T16 (and T14): 0.7 mA (neglecting the current of T15 and that of the divider R6 – R7).
3. The operation class of the power amplifier is set by the circuit of T14 (R6 = 4.5 k; R7 = 7.5 k):

$$2V_B = 0.6(R6 + R7)/R7 = \ldots = 0.96 \text{ V}$$

This is greater than the double of the BE threshold voltage (2 [0.35…0,4] = 0.7…0.8 V), but smaller than $2 \cdot 0.6 = 1.2$ V, thus the setting is class AB.

AC operation:

Input differential amplifier

On both sides, the transistors T1 – T3, that is T2 – T4 are in complementary Cascode arrangement, but the base of T3 and T4 (which are lateral pnp transistors) is not directly grounded, they become virtually grounded only in case of pure differential mode input signals. In such a case the input differential mode voltage is divided among 4 transistors, so the current change in either leg can be calculated by multiplying $v_{ind}/4$ with g_{21} (where g_{21} is the equal supposed trans-conductance of T1…T4). The T5 – T6 – T7 improved current mirror (R3 = 50 k) realises here phase addition, therefore the total trans-conductance of the input stage is the double of $g_{21}/4$:

$$G_{A1} = 2g_{21}/4 = 0.5g_{21} = 0.5 \cdot 15\mu A/26 \text{ mV} \sim 0.29 \text{ mS}$$

The maximum output current of the input stage is equal the sum of the operation point currents of the two input legs: $i_{out\ 1\ max} = 2 \cdot 15 = 30\ \mu A$

Input resistance (neglecting $r_{BB'}$):

$R_{ind} \approx 4(1 + ß)r_E \approx 4 \cdot 150 \cdot 26mV/15\mu A \approx 1$ Mohm (corresponding to the catalogue value)

We take the output resistance of the input stage infinite ($g_{22} = 0$): $R_{out\ 1} = \infty$.

When applying common input signals, the bases of T3 and T4 are not virtually grounded, and because they are connected to high a internal resistance point of the network the input transistors will not be driven by such input signals, meaning that the CMRR of the amplifier is very high (according to the catalogue CMRR = 70 …90 dB).

Offset-setting is possible by an external potentiometer. Since R1 = R2 = 1 k, a potentiometer with the value of 10 kohm can be used. (According to the catalogue the offset voltage is: 1 … 10 mV.)

Main amplifier (CE with Darlington pair of transistors):

The T15 – T16 Darlington works in common emitter connection without emitter degeneration, its load resistance is the parallel of the $1/g_{22}$ of T13 and the input resistance of the power amplifier (the latter depends on the load resistance R_L, but – since the T19 and T20 are high β transistors, the input impedance is high in case of the usual value of R_L in the order of magnitude of 1-10 k.

The input resistance of the main amplifier (calculating with β = 100: $h_{11(T16)} = 100 \cdot 26/0.7 = 3.7$ k):

$$R_{in\ 2} = 2\ h_{11(T15)} = 2 \cdot 100\ h_{11(T16)} = 740 \text{ k}$$

With this value, the voltage gain of the input stage:

$$A_{v1d} = G_{A1}\ R_{in\ 2} = 0.29 \cdot 740 = 215$$

The voltage gain of the main amplifier (taking the load resistance of the Darlington $[0.5(1/g_{22})]$ x $(h_{21}R_L) = 50$ k): $A_{v\ 2} = -(g_{21}/2)50 = -\ [(0.7/26)/2]50 = -\ 673$

Since the voltage gain of the power stage is practically $A_{v\ 3} \approx 1$, the overall differential voltage gain of the entire operational amplifier (the sign is not important, because it is determined by the use of the inverting or non-inverting input):

$$A_{vd} = A_{v1d}A_{v\ 2}A_{v\ 3} = 215 \cdot 673 = 145\ 000$$

From the catalogue: $A_{vd} = 20\ 000 \ldots 200\ 000$

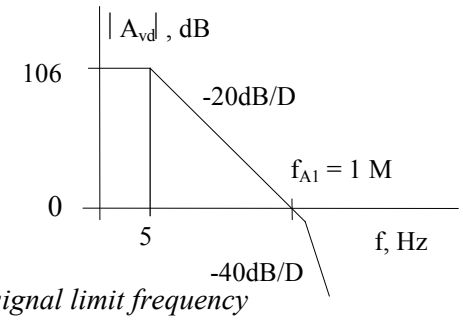
Frequency response: The capacitance $C_c = 30$ pF determines dominant time constant in the input circuit of the main amplifier. Transforming C_1 (Miller-effect): $C_1^* = (1 + 673)\ 30 = 20220$ p.

The resistive component of the time constant is $R_{in\ 2}$, thus the dominant break-point frequency:

$$\omega_{lh} = 1/20\ 220 \cdot 10^{-12}\ 740 \cdot 10^3 = 67 \text{ r/s, from where } f_{lh} = 10 \text{ Hz}$$

In the catalogue: 5 … 10 Hz.

Bode-plot of the voltage gain:



The notions slew rate and large signal limit frequency

- The slew rate (SR) is the maximum changing speed of the output voltage:
$SR = (\Delta V_{out}/\Delta t)_{max} = \Delta V_{C(T16)}/\Delta t = (i_{out\ 1\ max}\Delta t)/(C_c\Delta t) = i_{out\ 1\ max}/C_c = 30\mu A/30pF = 10^6 V/s = 1V/\mu s$
In the catalogue: 0.5 V/μs.

- The large signal limit frequency belongs to an output voltage amplitude, which corresponds to the maximum amplitude in the linearity range (approx. 10 - 12 V with $V_S = \pm$ 15 V):
$\omega_{lsl} V_{out\ p\ max} = SR \quad \Rightarrow \quad \omega_{lsl} = 10^6/10 = 10^5$ r/s $\quad \Rightarrow \quad f_{lsl} = 10$ kHz
In accordance with the catalogue.

Power amplifier:

Current limiting: $R_E = R9 = R10 = 25$ ohm, therefore the current limiting begins at an output current $i_{out\ max} = 0.4V/25$ ohm = 16 mA (operation principle: when the voltage across R_E reaches the threshold voltage of T17, that is T18, these transistors go into conduction and shunt away the current from the bases of the power transistors, and so the shunted current arrives to the output without having been multiplied by the β of these transistors and it is limited to the op-point current of the CE stage).
$R_{out} = 25 + R_B/h_{21} \approx 75$ ohm (from the catalogue, consequently e.g. in case of $\beta = h_{21} = 400$ we get a value for the resulting resistance in the base circuit of the power transistors $R_B = 20$ k).
Maximum output voltage swing: $v_{out\ p\ max} = V_S - 2V_{BE} - i_{out\ max} R_E = 15 - 2\ 0.6 - 0{,}4 = 13.4$ V
Linearity range: $v_{out\ p\ max\ lin} = 10 \ldots 12$ V (with some reserve)

Differences in case of 748 op. amp.

- the compensating capacitance is external,
- different offsetting in order to ensure a common pin point for the offsetting and the compensating elements..
Advantage: always the most favourable compensating capacitance can be chosen.
Disadvantage: the offsetting elements have greater values in the range 1 ... 10 Mohm introducing more noise and making the circuit more sensitive for disturbing effects.

End of class 16.